Software is Key

Intel MIC: GPU level performance with CPU level programmability

Jim Cownie <james.h.cownie@intel.com>
Intel
Optimization Notice

Intel’s compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice.

Notice revision #20110804
INFORMATION IN THIS DOCUMENT IS PROVIDED “AS IS”. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO THIS INFORMATION INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. Buyers should consult other sources of information to evaluate the performance of systems or components they are considering purchasing. For more information on performance tests and on the performance of Intel products, reference www.intel.com/software/products.


*Other names and brands may be claimed as the property of others.

Copyright © 2011. Intel Corporation.

http://intel.com/software/products
Who am I?
Overview

• History
  – Software
  – Benchmarking
  – Hardware

• Hardware Fundamentals
  – Moore’s Law
  – Energy

• Where are we now
  – Xeon
  – MIC

• Conclusions
### History: Software

**How old is HPC software?**

<table>
<thead>
<tr>
<th>Code</th>
<th>Area</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>NASTRAN</td>
<td>Structures</td>
<td>1968</td>
</tr>
<tr>
<td>Spice</td>
<td>E-Cad</td>
<td>1972</td>
</tr>
<tr>
<td>Pam-Crash</td>
<td>Structures</td>
<td>1978</td>
</tr>
<tr>
<td>UKMO Unified Model</td>
<td>Weather</td>
<td>1990</td>
</tr>
<tr>
<td>PETSc</td>
<td>Solvers</td>
<td>1991</td>
</tr>
<tr>
<td>LAPACK</td>
<td>Solvers</td>
<td>1992</td>
</tr>
<tr>
<td>NWCHEM</td>
<td>Chemistry</td>
<td>1995</td>
</tr>
<tr>
<td>WRF</td>
<td>Weather</td>
<td>2000</td>
</tr>
</tbody>
</table>

- Code lasts much longer than hardware
- We must support old code on new hardware
**History: Software**

**How old are languages?**

<table>
<thead>
<tr>
<th>Language</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fortran</td>
<td>1966 (FORTRAN 66)</td>
</tr>
<tr>
<td>C</td>
<td>1978 (K&amp;R)</td>
</tr>
<tr>
<td>C++</td>
<td>1985 (C++ Programming Language)</td>
</tr>
<tr>
<td>MPI</td>
<td>1994</td>
</tr>
<tr>
<td>OpenMP</td>
<td>1997</td>
</tr>
</tbody>
</table>

- Languages that work have a long life
  - Investment in code
  - Investment in brain-cells

- All have open specifications & many implementations
  - Formal standards (C, C++, Fortran)
  - Open industry standards (MPI, OpenMP)

- We must support old languages on new hardware
History: Old benchmarking tricks come around too...

How do you make an accelerator look good?

• Only time kernels, not the whole code
  – Even if I can offload 25% of the execution and have it run infinitely fast, that’s still only a 1.33x speedup

• When quoting speedup ignore data transfer time
  – or choose a benchmark with no data (e.g. Mandelbrot)

• Change the algorithm but don’t use the new one on the CPU
  – (Special case) Compare single precision results on the accelerator with double precision on the CPU

• Compare a newly released accelerator with a two year old CPU
History: Old benchmarking tricks come around too...

What’s the easiest way to get a good speedup?
• Start with something slow...
• So don’t optimize the CPU case
  – Use old or poor compilers and compile for an 8087
  – Only use a single core on the CPU even if it has twelve or more
  – Spend all your effort on the accelerator code
  – Assume that effort to rewrite code for the accelerator is free, but that there is no effort to do any tuning of the CPU code
### History: Hardware

<table>
<thead>
<tr>
<th>Hardware</th>
<th>Flops</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPS AP-120B</td>
<td>12 M</td>
<td>1976</td>
</tr>
<tr>
<td>Intel 8087</td>
<td>50 K</td>
<td>1980</td>
</tr>
<tr>
<td>ClearSpeed</td>
<td>25 G</td>
<td>2003</td>
</tr>
</tbody>
</table>

- The wheel of reincarnation turns
- Computing at the end of an I/O bus is **hard**
- Implementations which work end up on the CPU die
  - Moore’s law; we need something to use all the transistors profitably
  - 8087 moved into the CPU
  - SIMD vector floating point moved into the CPU (SSE, SSE2, AVX, AVX2, …)
  - Crypto instructions moved to the CPU (SPARC and Xeon AES-NI)
Fundamentals: Moore’s law is alive and well

New Intel technology generation every 2 years. Intel R&D technologies drive this pace well into the decade.

90nm 2003

65nm 2005

45nm 2007

32nm 2009

22nm 2011

Hi-K metal-gate

3-D Tri-gate

14nm 2013

10nm 2015

Shrink

We will have lots of transistors!
## Fundamentals: Energy

<table>
<thead>
<tr>
<th>Nvidia* energy numbers</th>
<th>2010 40nm</th>
<th>2017 10nm high freq</th>
<th>2017/2010</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP FMA</td>
<td>50 pJ</td>
<td>8.7 pJ</td>
<td>17%</td>
</tr>
<tr>
<td>3x64bit read, 1x64bit write in 8K SRAM</td>
<td>56 pJ</td>
<td>9.6 pJ</td>
<td>17%</td>
</tr>
<tr>
<td>Wire energy (256b,10mm)</td>
<td>310 pJ</td>
<td>200 pJ</td>
<td>65%</td>
</tr>
<tr>
<td>DRAM Access</td>
<td>10,000 pJ</td>
<td>1,700 pJ</td>
<td>17%</td>
</tr>
</tbody>
</table>

- ALU ops themselves are cheap
- Locality (even on die) is important, and becomes critical in the future
  - Caches matter
  - A streaming architecture will not scale forward
Where are we now?

• Hardware Convergence
  – Mainstream chips have multiple cores and SIMD vector units (AVX: 256 bits (8 float, 4 double); MIC: 512 bits)
  – GPU hardware is acquiring normal CPU features so that it is easier to program
    – Caches
    – Subroutine calls

• Accelerators move on die
  – Off die is too slow
  – Accelerator should be in process’s address space
  – We have all those transistors to use
Intel’s Many Core and Multi-core Engines

Die Size not to scale

Multi-core Intel® Xeon® processor at 2.26-3.5 GHz

Many Integrated Cores at 1-1.2 GHz

Intel Xeon processor:
• Foundation of HPC Performance
• Suited for full scope of workloads
• Industry leading performance/watt for serial & parallel workloads.

MIC processor:
• The performance of a highly parallel processor
• The benefits of familiar, standard programming models
Xeon: Intel® Advanced Vector Extensions (Intel® AVX)

- 2X the throughput of SSE
- Extend SSE FP instruction set to 256 bits operand size
  - Intel AVX extends all 16 XMM registers to 256bits (8 single-precision, 4 double-precision)
- New, non-destructive source syntax
  - VADDPS ymm1, ymm2, ymm3
- New Operations to enhance vectorization
  - Broadcasts
  - Masked load & store
Max 152GF effective flops per socket, 91% efficiency on HP Linpack

172 peak Gflops / socket – 2x improvement with Intel® AVX

Industry’s first integrated PCI Express* 3.0

Source: Top500.org, November 2011
MIC: Knights Corner

- Exists in 22nm process
- > 50 cores/die
- 512 bit SIMD instructions
- Early Si delivers 1TFlop sustained on DGEMM
- Runs Linux
- Can be
  - a network node (ssh in...)
  - used as an offload processor over PCIe
- Targeted by Intel compilers
Invest in Common Tools and Programming Models

Multicore

Intel® Xeon® processors are designed for intelligent performance and smart energy efficiency

Continuing to advance Intel® Xeon® processor family and instruction set (e.g., Intel® AVX, etc.)

Code

Use One Software Architecture

Many-core

Intel® MIC Architecture - co-processors are ideal for highly parallel computing applications

Software development platforms ramping now

Use One Software Architecture Today. Scale Forward Tomorrow.
**Experience with Knights Ferry design and development kit**

- **Unparalleled productivity:** in under 3 months
  - Ported all of NWChem (chemistry), ENZO (astro.), ELK (mat. sci.), MADNESS (app. math.), MPI, GA, ...
  - Correct ports in less than one day each
  - Circa 5M LOC (Fortran 77/90, C, C++, Python)
  - MPI, Global Arrays, ...

- **Most of this software does not run on GPGPUs and probably never will due to cost and complexity**

- **Demonstrated execution modes:**
  - Native mode: KNF is fully networked Linux system
  - Offload mode: KNF is an attached accelerator
  - Reverse offload mode: KNF in native mode offloads to host
  - Cluster mode: parallel application distributed across multiple KNF and hosts using MPI
MIC: Achieving Performance

• Parallelize code
  – Reduce serial code as much as possible
  – Minimize critical sections
  – Improve load balance (or use a model that handles it)

• Vectorize code
  – Loop transformations
  – Vectorization directives/pragmas
  – Reductions

• Memory hierarchy optimizations
  – Blocking, Cache-Oblivious algorithms, ...

• Use existing tools on Xeon

• All of these benefit code on CPUs as well
  – Doing them now is worthwhile
  – MIC is just more “extreme”, or “focused”
Depressing Conclusions

• There are no silver bullets
• Data parallelism & vectorization is important for all of the current hardware
  – and will become more important in the future
• As it always has, new hardware requires tuning to achieve performance
  – Unfortunately, using the same programming language doesn’t mean performance is portable
• As a community we forget our history and love the new
  – Vectorization is “so 1970’s” no-one would publish a paper on that nowadays
  – Papers on tuning are hard to publish, yet it’s easy to publish papers on rewriting code in “language du jour”
Cheerful Conclusions

• There are no silver bullets
  – We’ll all be in work for a while yet!
• You don’t have to use new programming languages
  – Fortran, C, C++,… can all be used
  – Parallelism can be expressed with OpenMP, TBB, Cilk™Plus, pthreads (if you must), MPI, …
• Improving code for data and thread parallelism is not wasted work
  – It pays off on the CPU as well as on accelerators
• There is much more public information on MIC available, for instance
  • **Highly Parallel Applications and Their Architectural Needs**
  • **Fast Sort on CPUs, GPUs and Intel MIC Architectures**
• Remember, Google Is Your Friend.
Other benchmark cheats

• Less relevant for GPU, but for parallel...
  – Compare internal speedups, not absolute speeds.
Amdahl was Smart

- Amdahl’s law is useful for thinking about accelerators as well as parallelism
  - Treat the accelerated portion of the code as if it were parallel
  - Use the accelerator kernel speedup as the parallel section speedup (“Nprocessors”)
  - Out pops the overall speedup
  - For a better estimate include the data transfers
  - Easily gives “speed of light” numbers (set offload kernel time to zero)
Slide 4: Picture from http://en.wikipedia.org/wiki/File:Daniellion.jpg “This image (or other media file) is in the public domain because its copyright has expired. This applies to Australia, the European Union and those countries with a copyright term of life of the author plus 70 years.”

Slide 6: Dates are as close to release 1.0 as I can find. Sources below
http://en.wikipedia.org/wiki/LAPACK
http://en.wikipedia.org/wiki/Pam-Crash
http://www.metoffice.gov.uk/research/modelling-systems/unified-model
http://www.mmm.ucar.edu/mm5/mpp/ecmwf01.htm

Slide 12: Energy numbers from Nvidia

Slide 13: Die picture shows that the CPU is not the largest thing on the die. Compare the area of the graphics with the four cores. Total graphics ~= Total Cores.
Cores are certainly < 50% of the die.


Slide 19: From NICS SC11 presentation, video at http://www.youtube.com/watch?v=TOVokMC1r5g makes the same points but doesn’t include this exact slide...

Slide 20: Programming models that handle imbalance are things like Cilk™Plus or TBB, as against OpenMP’s default static scheduling