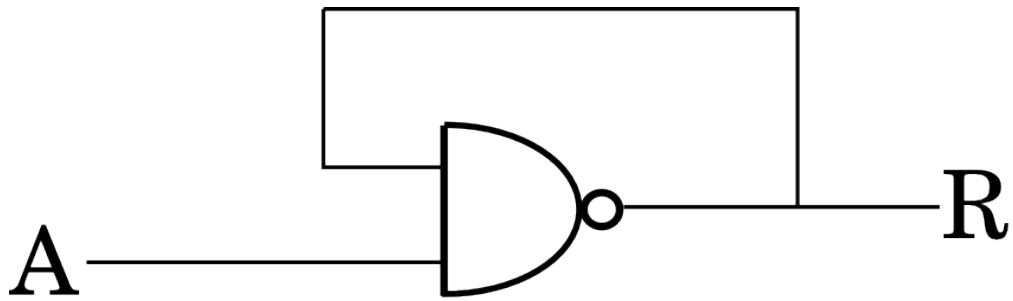
Lecture 6

Time-Dependent Behaviour of Digital Circuits with Feedback

In this lecture we will:

- Examine the behaviour of a digital circuit in which connections between gate outputs and inputs create a loop which we call feedback.
- Remember, it is perfectly legal to connect any gate output to any gate input as long as outputs are not connected together.
- $\cdots$ knowing this, student V. Mischievous presented me (on paper) the following circuit:

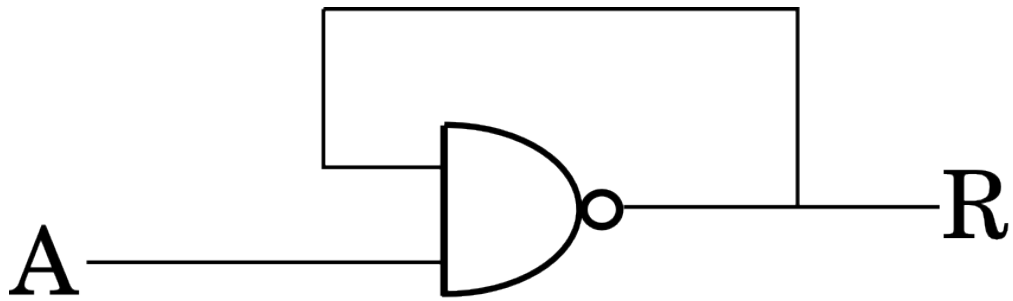
A Curious Circuit



What is the output of this circuit?

If input A is logic 0, R is logic 1, [0, 1] input to a NAND gate produces logic 1 and R is logic 1 ··· ok ···

A Curious Circuit



What is the output of this circuit?

If input A is logic 1, Boolean algebra tells us:

$$R = (R.A)' = (R.1)' = R'$$

Impossible! Now what do we do??????

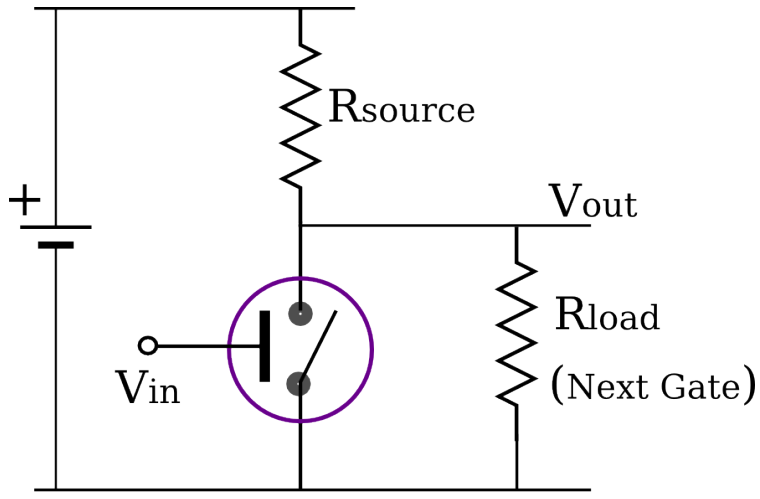
Engineering Approach

When a model (like the Boolean algebra model of a digital gate) breaks down, and its behaviour is unpredictable, we must go down one ”physical description” level and examine how the actual physical device was constructed.

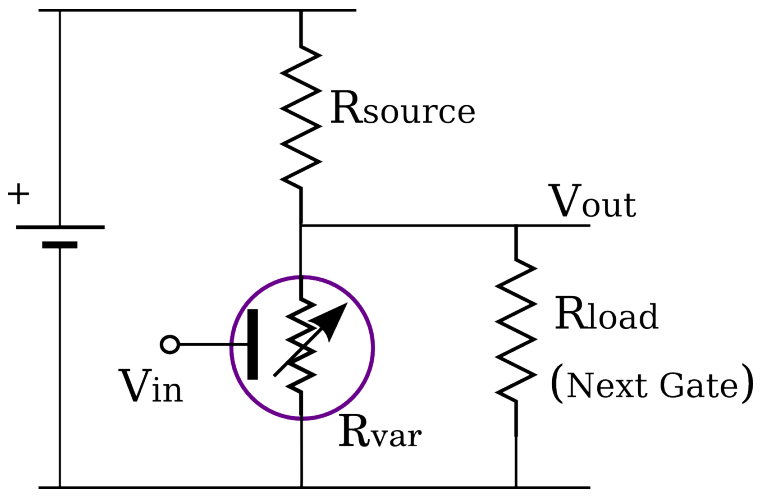
This may help us to predict what will happen.

So what were those models from the last lecture?

Quasi-Physical Models



Switch and Delay

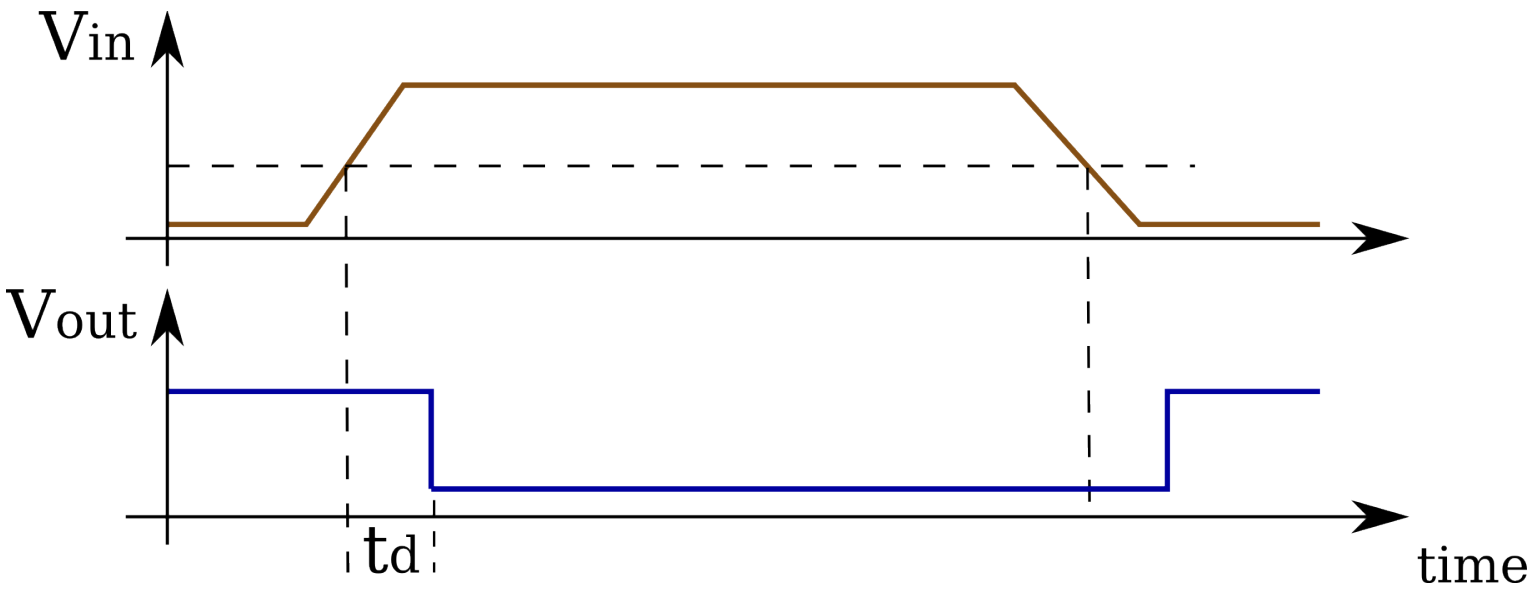


Resistance and Capicitance

These are needed to construct a logical model which can be used to analyse unusual behaviour in the laboratory.

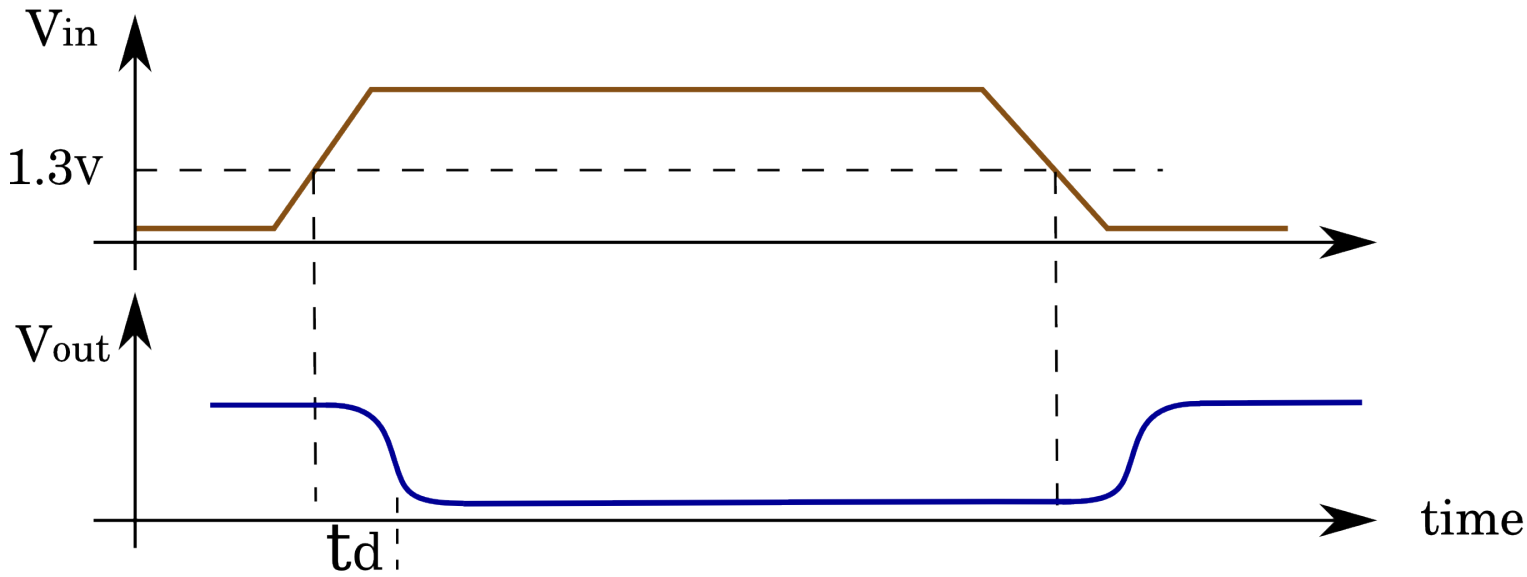
The Switch and Delay Model

This model only really differs from Boolean algebra by the inclusion of a time delay between input (left hand side) and output (right hand side). Its time behaviour is described by the following example:



The resistance capacitance model

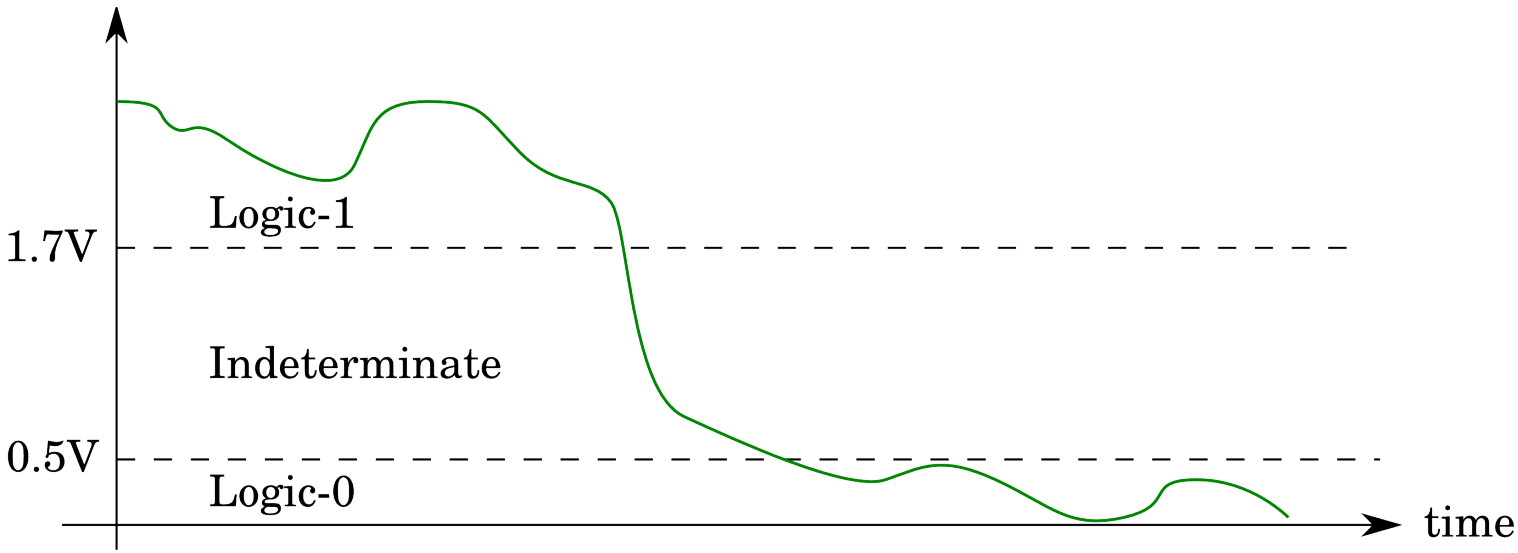
This gives us a more accurate representation of the real behaviour



We no longer have a valid Boolean signal output when changing from 0 to 1 and back.

Analogue Electronics

The variable resistance/capacitance model is not digital but analogue. The variable resistor can be adjusted continuously. To interpret its behaviour as a digital circuit we need to introduce the concept of a noise margin.



Noise Margin

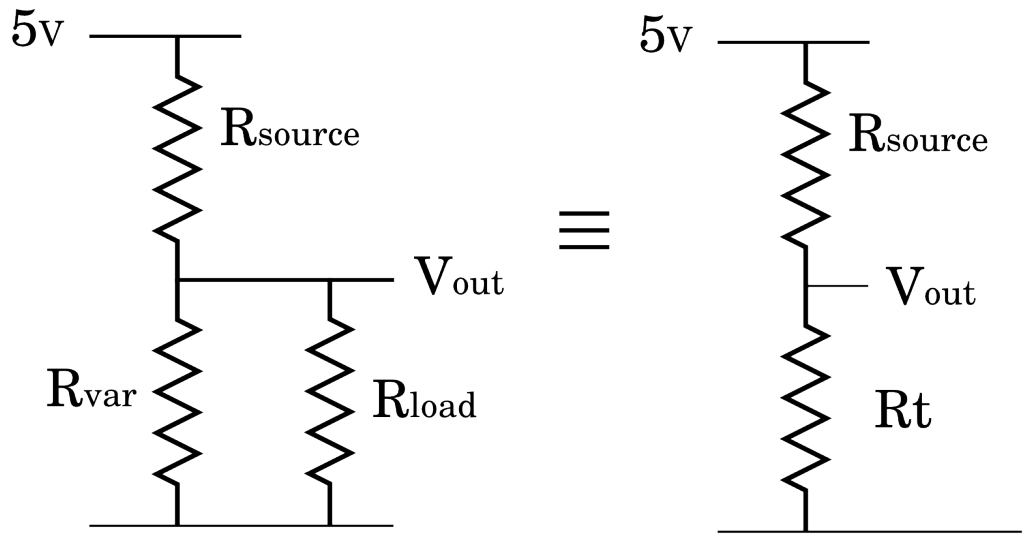
The noise margin gives us a definite threshold (1.7volts) above which we know that our signal represents a Boolean 1, and similarly a definite threshold (0.5Volts) below which we know our signal represents Boolean 0.

We aim to design our circuits so that they operate well away from the threshold, so normally we aim to make Boolean 1 around 3.5 Volts, and Boolean 0 around 0.3 Volts

So how do we determine the output voltage?

Potential Dividers

The variable resistance model acts like a potential divider. So:

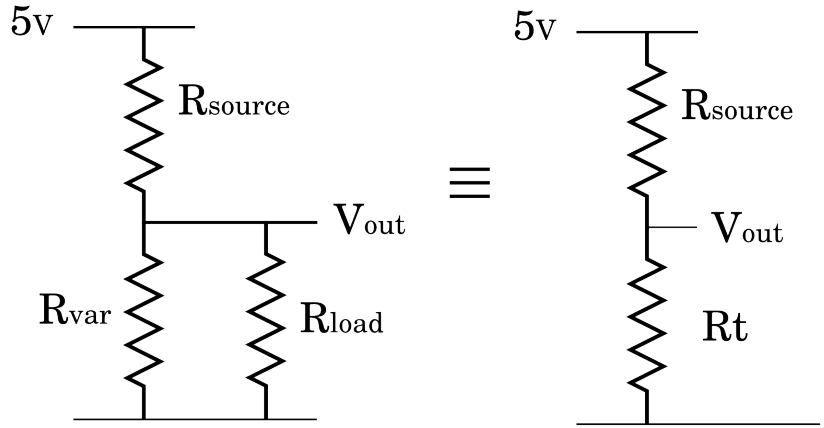


$$\frac{1}{R_t} = \frac{1}{R_{var}} + \frac{1}{R_{load}} \qquad V_{out} = \frac{5R_t}{R_{source} + R_t}$$

R_{load} is the combined resistance of all the gates to which the transistor is connected.

Putting in some real resistances

$$\frac{1}{R_t} = \frac{1}{R_{var}} + \frac{1}{R_{load}}$$



If an inverter is connected to one other gate the typical resistances and voltages are:

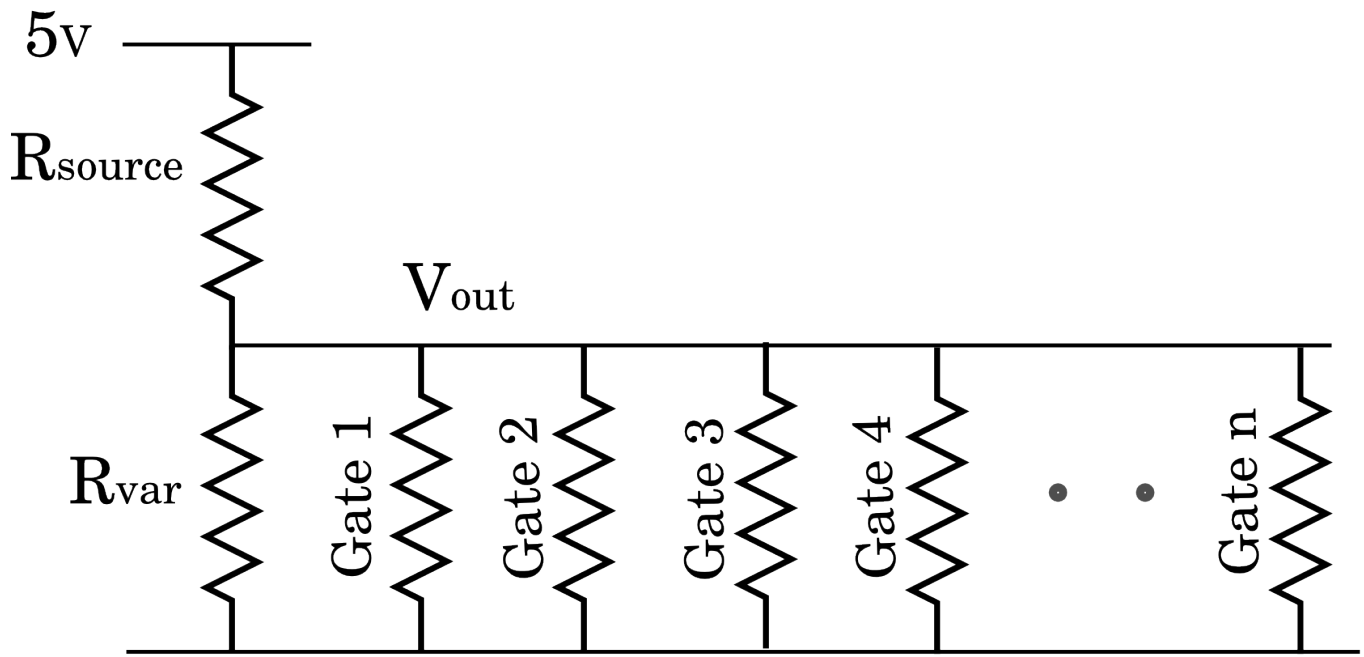
	$R_{source}(\Omega)$	$R_{load}(\Omega)$	$R_{var}(\Omega)$	$R_t(\Omega)$	V_{out} (Volts)
Logic-1	1000	10000	3000	2308	3.5
Logic-0	1000	10000	60	59	0.28

The gate works well with good noise margins.

Fan-Out

The fan-out of a gate is the number of different gate inputs to which it is connected.

If a transistor is connected to n gates, the circuit becomes:



Fan-Out

Resistors in parallel combine according to the inverse law:

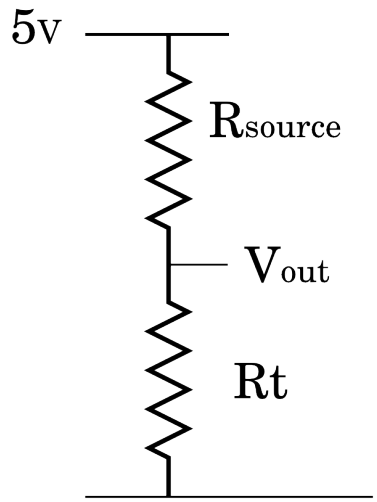
$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \cdots \frac{1}{R_n}$$

So if a gate output is connected to 10 gate inputs the load resistance R_{load} becomes 1/10 of a single gate. The operating voltages become:

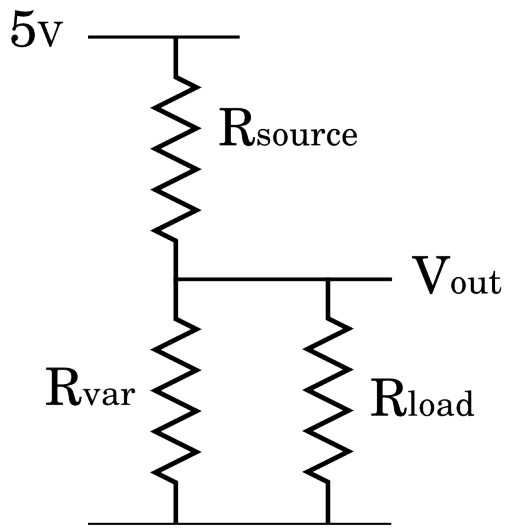
	$R_{source}(\Omega)$	$R_{load}(\Omega)$	$R_{var}(\Omega)$	$R_t(\Omega)$	V_{out} (Volts)
Logic-1	1000	1000	3000	750	2.1
Logic-0	1000	1000	60	57	0.27

Problem Time!

Given that $R_{source} = 1000$ Ohms, estimate the value of R_t when the circuit will fail, ie when the output voltage corresponding to Boolean 1 will be below 1.7.



Given $R_{var} = 3000$ Ohms for logic 1 and $R_{load} = 10000$ Ohms for a single gate (fan-out=1), estimate the fan-out that will cause a failure.



Solution 1

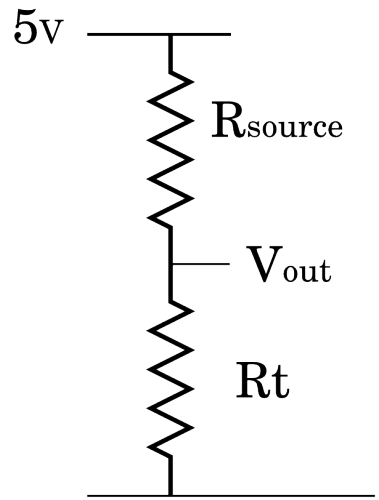
The output voltage is calculated by a potential divider.

$$V_{out} = 5 \times \frac{Rt}{R_{source} + R_t} = 1.7$$

$$(5 - 1.7)R_t = 1.7R_{source}$$

$$R_t = (1.7/3.3)R_{source} \approx R_{source}/2$$

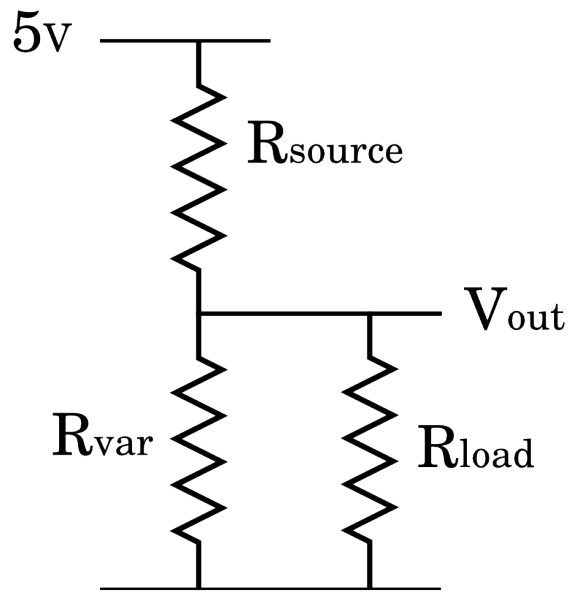
R_t is approximately 500 Ohms



Solution 2

$$\frac{1}{R_{load}} + \frac{1}{R_{var}} = \frac{1}{R_t}$$

From the previous problem we know that $R_t = 500$ Ohms causes failure.



$$\frac{1}{R_{load}} + \frac{1}{3000} = \frac{1}{500}$$

$$R_{load} = 600$$

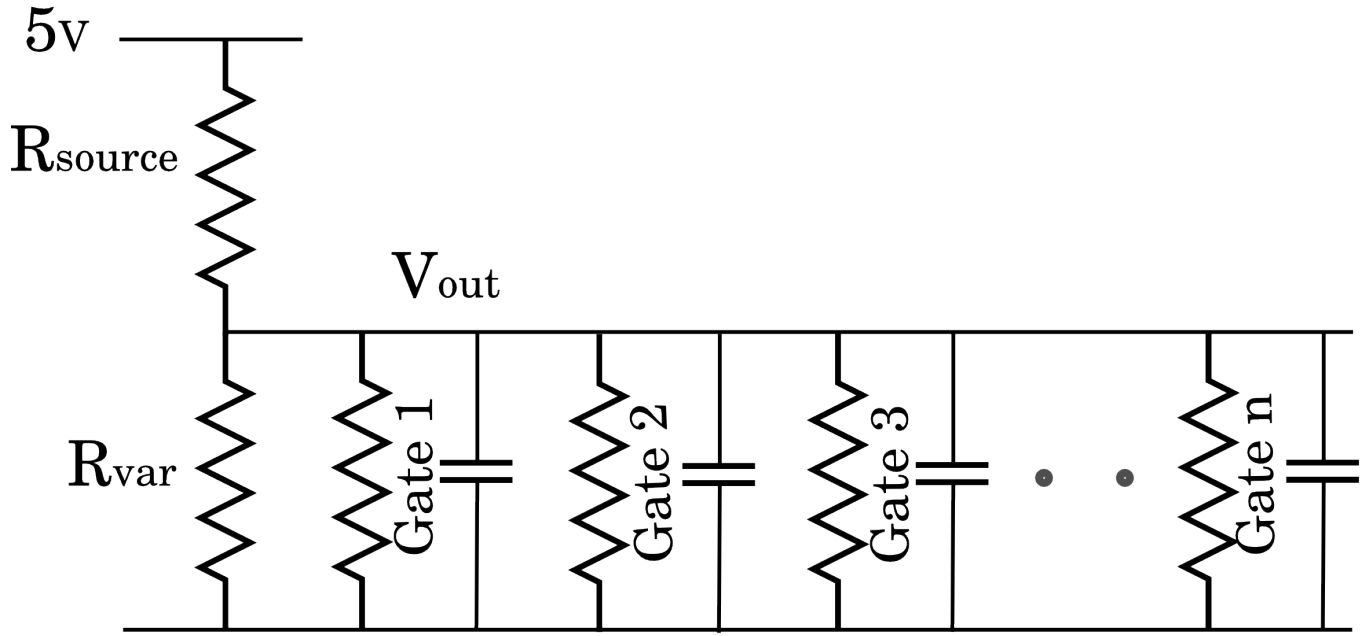
For a fan out of n, $R_{load} = 10000/n$

So $n = 10000/600 \approx 17$

Fan-Out

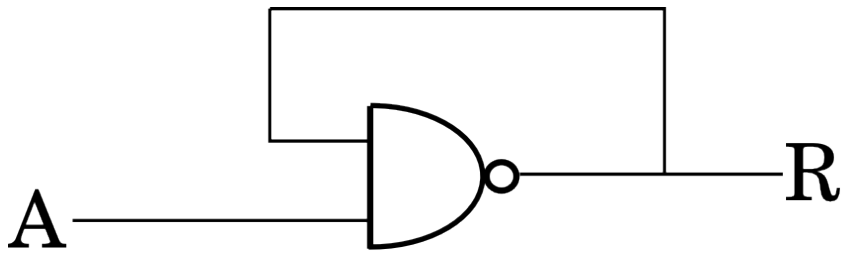
Another undesirable property of large fan-outs is that the time delay increases because the load capacitor increases.

Time delay is directly proportional to the size of the load capacitor. Capacitors in parallel add.



Returning to the curious circuit:

Analysis using the Switch-and-Delay Model



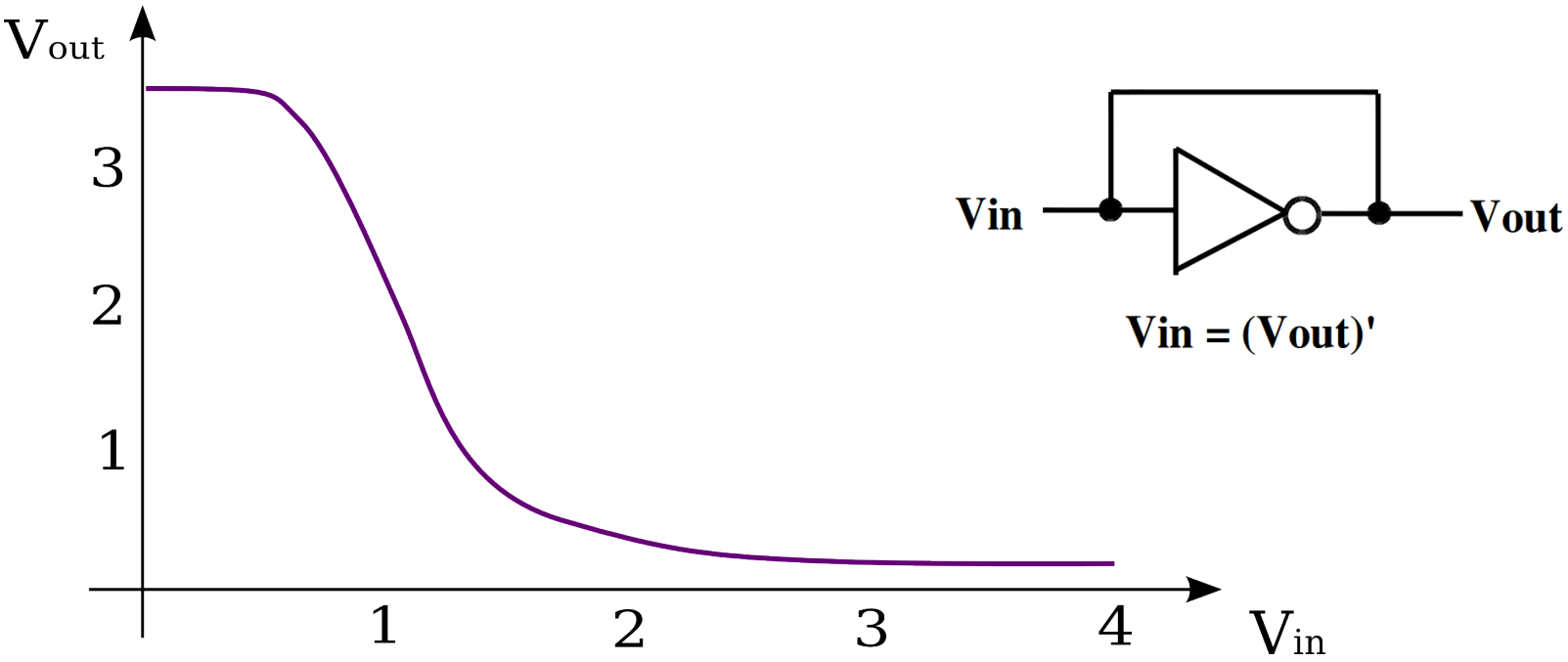
Let A=1, and assume R=1 initially:

- The gate senses inputs 11 and waits a bit (delay!)
- The output stage switches to the correct output: R=0
- The gate senses inputs 01 and waits a bit (delay!)
- The output stage switches to the correct output: R=1

$\cdots$ and so on $\cdots$ we have oscillation.

Analysis using the Variable Resistor Model

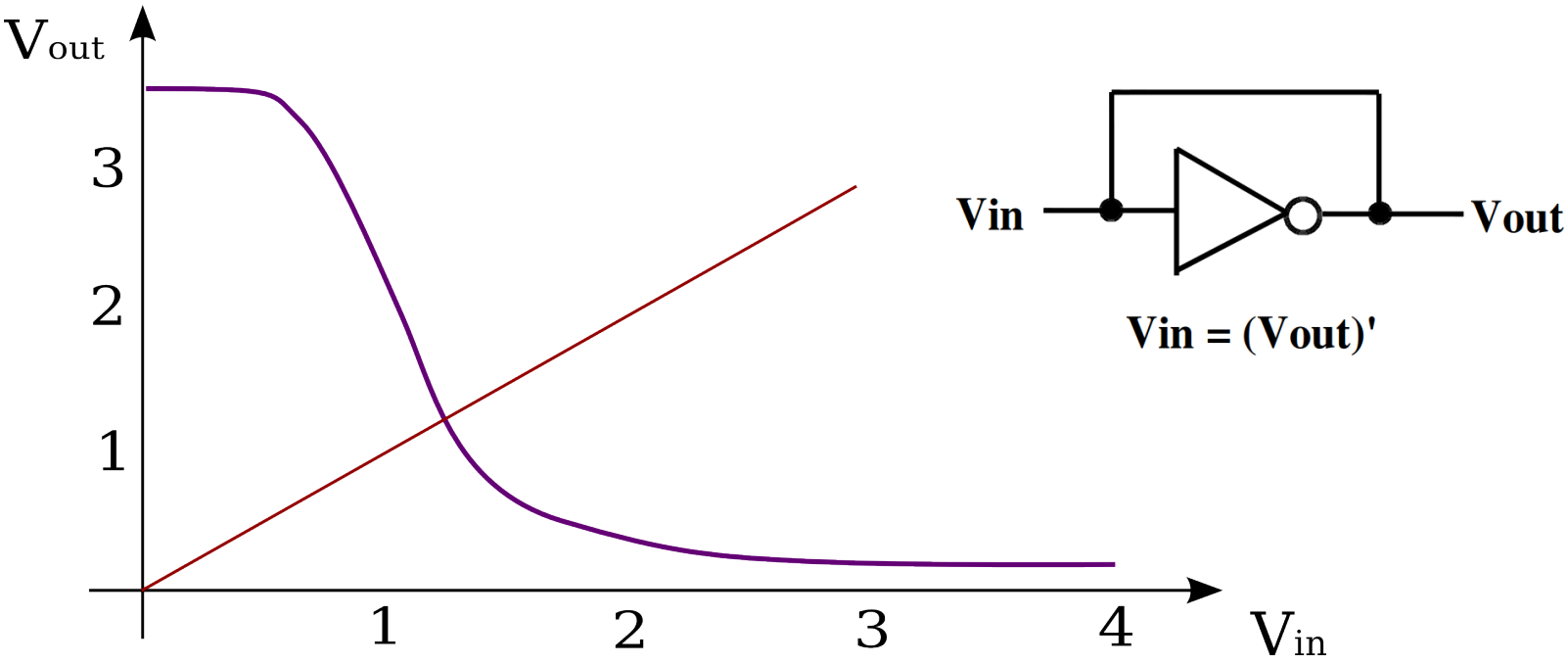
With the input A=1 the NAND gate is equivalent to an inverter.



Vin = (Vout)'

Analysis using the Variable Resistor Model

We CAN solve this impossible looking problem graphically, since Vin=Vout represents a straight line through the origin.



What this model says is that the output of this circuit will settle at an invalid digital value around 1.2 volts.

So, what will happen in the lab?

The variable resistor model is the more accurate of the two, so the most likely result is that the circuit output will be a constant 1.2 Volts.

However, we do not not know for certain unless a very very very high frequency oscilloscope is connected to the output of the circuit. Any oscillation will be very fast and difficult to detect.

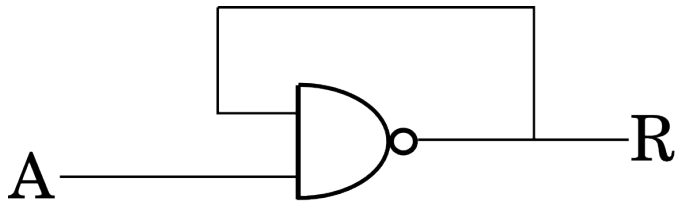
There are more accurate physical models of the transistor - but for the time being we will stick with the simplest - switch-and-delay

Digital Circuits with Feedback

The curious circuit is an example of Feedback. We will look at more useful circuits with feedback. To analyse their behaviour we will:

1. Assign names to the independent inputs of the circuit and to all its gate's outputs.
2. Create a table with two columns of numbers. The first column is labelled NOW and has all the possible combinations of 1s and 0s for the independent inputs and the gate outputs.
3. The second is labelled NEXT and will contain the new values of the gate outputs after a time delay.

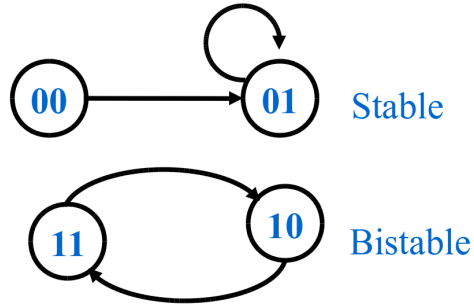
Analysing Circuits with Feedback



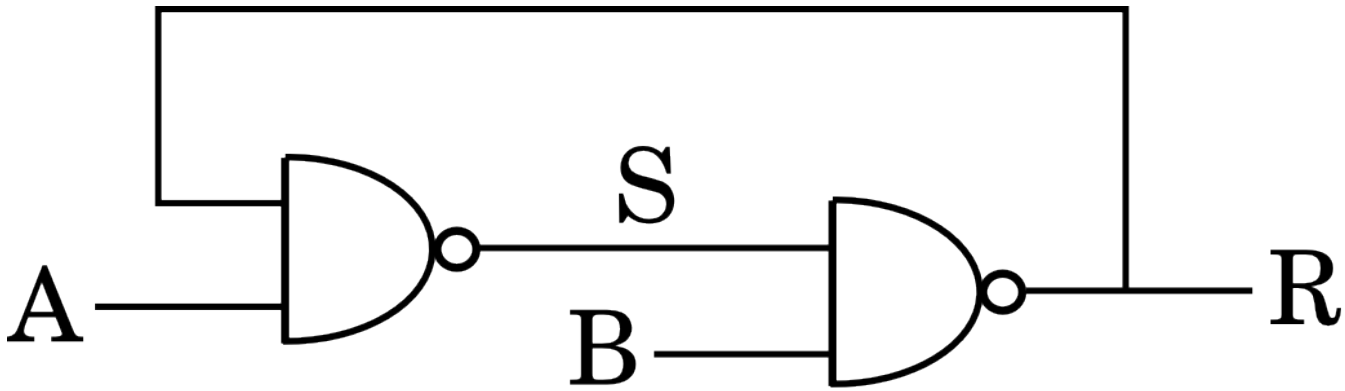
Transition Table

NOW	NEXT
A R	A R
0 0	0 1
0 1	0 1
1 0	1 1
1 1	1 0

Transition Diagram



Analysis of a More Useful Circuit



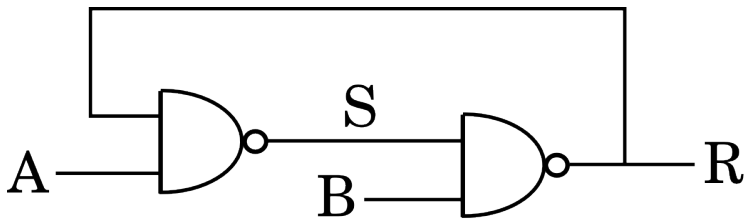
The Boolean Equations for this circuit are:

$S = (A.R)'$ $R = (S.B)'$

We have four variables so there will be sixteen states.

Building the Transition Table

We find the transition table from the circuit

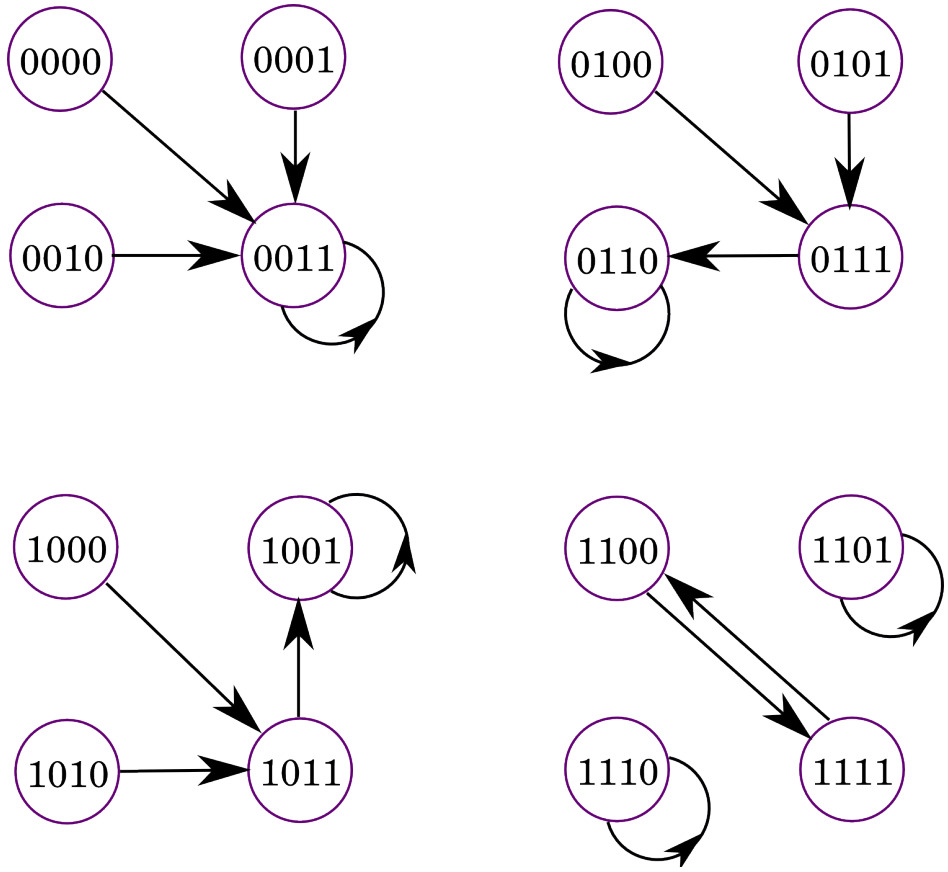


Stable states are highlighted in blue

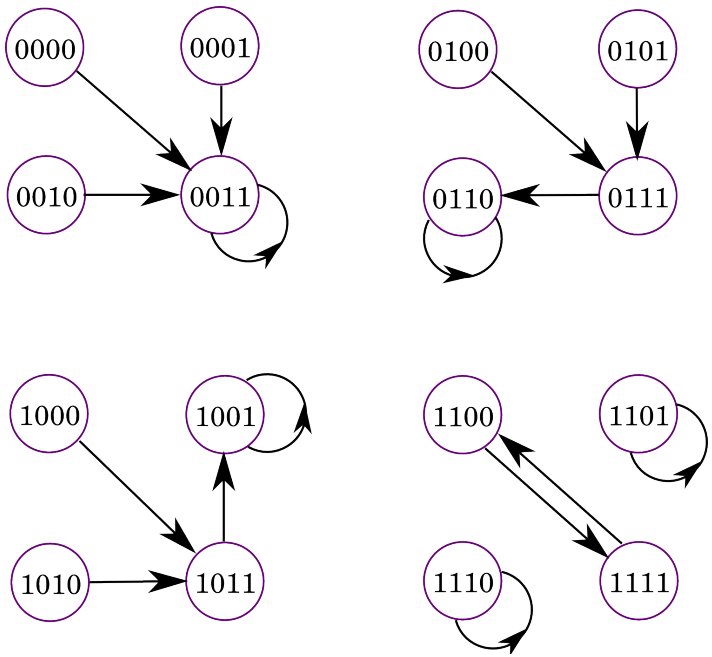
NOW				NEXT			
A	B	S	R	A	B	S	R
0	0	0	0	0	0	1	1
0	0	0	1	0	0	1	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	1
1	0	1	1	1	0	0	1
1	1	0	0	1	1	1	1
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	0	0

Building the Transition Diagram

NOW				NEXT			
A	B	S	R	A	B	S	R
0	0	0	0	0	0	1	1
0	0	0	1	0	0	1	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	1
1	0	1	1	1	0	0	1
1	1	0	0	1	1	1	1
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	0	0



Circuit Behaviour



From the diagram we see the following:

- Input 00 $\rightarrow$ Output 11
- Input 01 $\rightarrow$ Output 10
- Input 10 $\rightarrow$ Output 01
- Input 11 $\rightarrow$ Hold or oscillate

Next time we will use this to make a memory circuit.