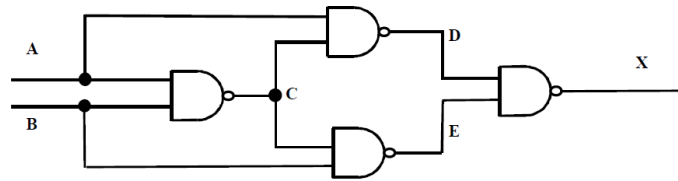


Tutorial 4: Timing in Logic Circuits

Consider the following famous circuit:



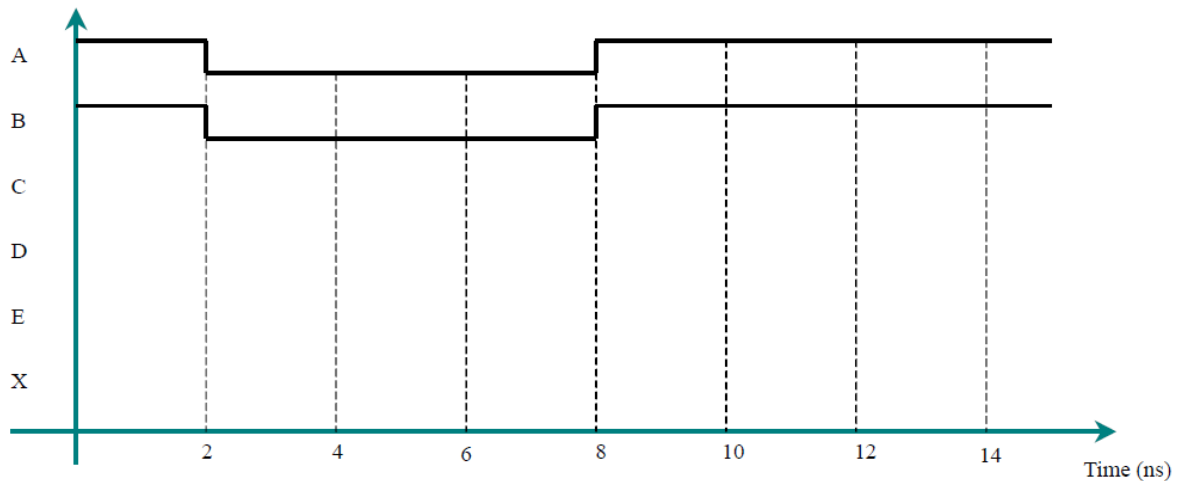
Problem 1

1. Using the simple switch model (ie Boolean Algebra) construct a truth table to determine its function.

A	B	C	D	E	X
0	0				
0	1				
1	0				
1	1				

Problem 2

Now, assume the switch model has a time delay, and let the time delay for a two input NAND gate be 2ns (2×10^{-9} seconds). Complete the following timing diagram for the circuit:

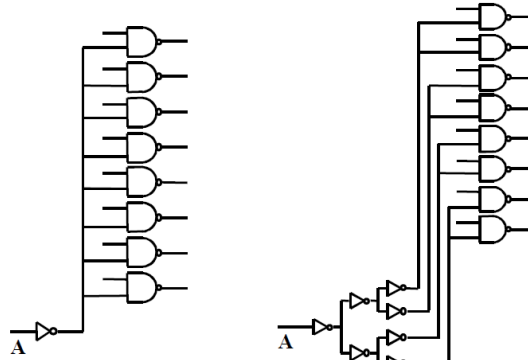


Problem 3

Assuming that an inverter causes a time delay of 1ns re-draw the circuit to remove the spike. Would this solution work if the inverters had a time delay of 0.95 ns rather than 1ns.

Problem 4

This is a difficult problem for those geniuses who understand physics. In our most complex model of the transistor we attributed the delay in switching a gate to the length of time it took to charge the capacitor between the gate and the drain. The input voltage to a gate is governed by the equation $V = 5(1 - \exp(-t/RC))$.



Using this model, and assuming that:

1. the input capacitances of all gates are the same
2. the gates all switch at about the same voltage level eg 1V for logic 1

determine which of the two implementations of an eight way buffer circuit will be the faster.