Learning Outcomes

At the end of this lecture you should
- Understand how gates can be integrated onto chips (ICs)
- Know the basic chip sizes – SSI, MSI, LSI, VLSI
- Comprehend how circuits can be used for data selection/movement
- Understand multiplexers, decoders and arithmetic logical units
- See how basic memory units can be integrated to make memory chips
- Have a grasp of how a microprocessor could be put together

Integrated Circuits

- All ICs (chips) are made up of logic gates
- These are square pieces of silicon onto which logic gates have been deposited
- Generally two rows of pins enable connection onto a larger circuit

IC - sizes

<table>
<thead>
<tr>
<th>Name</th>
<th>Abbreviation</th>
<th>Number of Gates</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small Scale Integrated</td>
<td>SSI</td>
<td>1-10</td>
</tr>
<tr>
<td>Medium Scale Integrated</td>
<td>MSI</td>
<td>10-100</td>
</tr>
<tr>
<td>Large Scale Integrated</td>
<td>LSI</td>
<td>100-100,000</td>
</tr>
<tr>
<td>Very Large Scale Integrated</td>
<td>VLSI</td>
<td>&gt;100,000</td>
</tr>
</tbody>
</table>
Example SSI Chips

7400 - Nand Gates

7404 - hex inverter

The 7400 TTL series

Example Circuit with SSI/MSI Chips

MSI Chips – the multiplexer

The 3 inputs A, B, C select which of the input lines is copied through to the output, f

In general, a multiplexer has $2^n$ inputs and n control lines and one output

Fits nicely into a 14-pin package (with ground and +5V)
A decoder has \( n \) inputs and \( 2^n \) outputs. Only one output is 1 – the one selected by the \( n \)-bit binary input number – the rest are zero.

Useful in transmitting line selection with fewer wires (e.g. selecting a memory chip).

The shifter. With \( c=0 \) shift left, \( c=1 \) shift right (remember that shift operations multiply or divide by 2).

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The comparator returns 1 if the two n-bit inputs A and B are equal, 0 otherwise.

The Arithmetic Logical Unit (ALU)

The ALU is able to perform multiple functions. Depending on the input to the decoder (F0,F1) one of four functions is selected – A and B, A or B, not B, arithmetic A+B.
8-bit ALU

We can link together 1-bit ALUs to form a multi-byte ALU (sometimes known as bit-slice circuits)

Extra not – tri-state buffers

The output is equal to the input if the control line is 1, otherwise it is disconnected.

Tri-state buffer (a) non-inverting, (b) effect when control is 1, (c) effect when control is 0 and (d) inverting version

Memory – the D-type latch

Memory chips

The memory chip shown here comprises 12 D-latches in a 4x3 configuration.

The 3 bit data will be read or written to one of the four words selected by the input lines \( A_0/A_1 \).

\( A_0/A_1 \) are the address lines and \( I_n/O_n \) are the input/output data lines
Memory Chips

• In fact, input and output are never used at the same time.
• Chips use the same pins for input and output

Larger memory chips – potential layouts

CPU design - VLSI

Summary

- Have shown how gates can be integrated onto chips
- Shown examples of SSI, MSI chips
- Comprehend how circuits can be used for data selection/movement (multiplexers/decoders)
- Understand multiplexers, decoders and arithmetic logical units
- See how basic memory units can be integrated to make memory chips
- Described how addressing can work at the electronic level
- Hopefully this gives a feel for how a VLSI microprocessor could be put together
This lecture - feedback

- The pace of the lecture was:
  A. much too fast  B. too fast  C. about right  D. too slow  E. much too slow

- The learning objectives were met:
  A. Fully  B. Mostly  C. Partially  D. Slightly  E. Not at all