Jacky (Wai Kit) Wong

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EDUCATION

Imperial College London — London, United Kingdom

- *Ph.D. in Department of Computing* — Sept. 2029
  - Supervisor: Paul H Kelly (Software Performance Optimisation Group)
  - Topics: Computer Architecture, Data Prefetching, Memory Systems
  - Full Scholarship as Doctoral Teaching Scholar
- *MEng in Electrical and Information Engineering* — Jun. 2024
  - Graduate with First Class Honors

Shen Wai International School — Shenzhen, China

- *International Baccalaureate Diploma Program* — Jun. 2020
  - Graduate with Honors: 41/45

WORK AND RESEARCH EXPERIENCE

Software Performance Optimisation Group, *Imperial College London* — London, United Kingdom
Postgraduate Researcher — Oct. 2024 – Present

- Attempting to prove and characterize prefetcher training interference, where the choices of the current selected prefetcher might destructively interfere with the training of other prefetcher candidates in a composite data prefetching system.
- Utilised Bayesian Optimisation to tune gem5 parameters to minimise both energy and performance for a specific program.

Final Year Project, *Imperial College London* — London, United Kingdom
A Coverage-Guided Tournament Approach to Composite Data Prefetching — Oct. 2023 – Jun. 2024

- Established a method of measuring the complementarity of data prefetchers using the percentage overlap of their proposed prefetch targets in gem5.
- Illustrated the potential for a tournament prefetcher scheme by showing significant performance gains when always choosing an optimal prefetcher offline.
- Demonstrated that coverage, a runtime metric measuring the percentage of cache misses the prefetcher was able to prevent, can predict the top prefetcher in 88.9% of tests.
- Developed an in-flight implementation in gem5, leading to on average 8.20% and at maximal 35.7% IPC uplift compared to baseline in CoreMark Pro.

Doctoral Teaching Programme, *Imperial College London* — London, United Kingdom
Graduate Teaching Assistant — Oct. 2024 – Present

- Assisting the department in core teaching roles, including interacting with students, coursework planning, coursework marking, performing code review sessions, and developing new labs and exercises.

Silicon Engineering Group, *Apple Inc.* — Swindon, United Kingdom
PMU Design Verification Intern — Apr. 2023 – Oct. 2023

- Contributed significantly to the triage and verification of a PMU project, maintained and extended the testbench structure, focusing on Security and Bus related designs. Resulted in a tape-out regression pass rate of over 99.5%.
- Developed a template-based tool for automatically generating System Verilog QDI (quasi delay insensitive) FSM test benches from the specification source.
- Developed several tools for monitoring design stability and verification completeness.

Undergraduate Research Opportunity Program, *Imperial College London* — London, United Kingdom
Team Member and Undergratuate Teaching Assistant — Jul. 2022 – Sept. 2022

- Reshaped and modernized the Instruction Architecture and Compiler senior year course by targeting RISC-V and building a RV32I compliant CPU with cache and exception handling using System Verilog, lead by Professor Peter Cheung.

SKILLS AND INTEREST

- Technical Skills: Gem5, System Verilog, Verilator, UVM, SVA, C++, Python, Linux, Bash, Quartus Prime.
- Language Skills: First Language: English, Mandarin (Chinese); Conversational Cantonese (Chinese).
- Personal Interests: PC hardware enthusiast, Ukulele, Chess, Chinese Drama, Home Cook.