

Computing Platform". IEEE Transactions on Computers (TC) (submitted).

3. Y.M. Lam, K.H. Tsoi and W. Luk. "*Parallel Neighbourhood Search on Many-cores Computing Platforms*". International Journal of Computational Science and Engineering (IJCSE) (submitted).
4. K.W. Kwok, K.H. Tsoi, V. Vitiello, J. Clark, C.T. Chow, W. Luk and G.Z. Yang. "*Dimensionality Reduction in Controlling Articulated Snake Robot for Endoscopy under Dynamic Active Constraints*". IEEE Transactions on Robotics (T-RO) (submitted).
5. K. H. Tsoi and W. Luk. "*Power Profiling and Optimization for Heterogeneous Multi-Core Systems*". ACM SIGARCH Computer Architecture News, vol.39, no.4, pp.8-13, Sept. 2011.
6. A.H.T. Tse, D.B. Thomas, K.H. Tsoi and W. Luk. "*Efficient Reconfigurable Design for Pricing Asian Options*". ACM SIGARCH Computer Architecture News, vol.38, no.4, pp.14-20, Sept. 2010.
7. K.H. Tsoi, A.H.T. Tse, P. Pietzuch and W. Luk. "*Programming Framework for Clusters with Heterogeneous Accelerators*". ACM SIGARCH Computer Architecture News, vol.38, no.4, pp.53-59, Sept. 2010.
8. K.H. Tsoi, K.H. Leung and P.H.W. Leong. "*A High Performance Physical Random Number Generator*". IET Proc. Computers & Digital Techniques, vol.1, no.4, pp.349-352, July 2007.

Conference papers:

9. S. Denholm, K. H. Tsoi, P. Pietzuch and W. Luk. "CusComNet: A Customisable Network for Reconfigurable Heterogeneous Clusters". In Proc. International Conference on Application-specific Systems, Architectures and Processors (ASAP), pages 9-16, 2011.
10. X.Y. Niu, K. H. Tsoi and W. Luk. "Reconfiguring Distributed Applications in FPGA Accelerated Cluster with Wireless Networking". In Proc. International Conference on Field Programmable Logic and Applications (FPL), pages 545-550, 2011.
11. K. H. Tsoi and W. Luk. "Power Profiling and Optimization for Heterogeneous Multi-Core Systems". In Proc. International Workshop on Highly Efficient Accelerators and Reconfigurable Technologies (HEART), 2011.
12. Y. Yamaguchi, K. H. Tsoi and W. Luk. "FPGA-Based Smith-Waterman Algorithm: Analysis and Novel Design". In Proc. International Symposium on Applied Reconfigurable Computing (ARC), pages 181-192, 2011.
13. Y. Yamaguchi, K. H. Tsoi and W. Luk. "A comparison of FPGAs, GPUS and CPUS for Smith-Waterman algorithm". In Proc. Field Programmable Gate Arrays (FPGA), poster, 2011.
14. A.H.T. Tse, D.B. Thomas, K.H. Tsoi and W. Luk. "Dynamic Scheduling Monte-Carlo Framework for Multi-Accelerator Heterogeneous Clusters". In Proc. IEEE Symposium on Field-Programmable Technology (FPT), pages 233-240, 2010.
15. V. Sriram, D. Cox, K. H. Tsoi and W. Luk. "Towards an embedded biologically-inspired machine vision processor". In Proc. IEEE Symposium on Field-Programmable Technology (FPT), pages 273-278, 2010.
16. Q. Liu, T. Todman, K. H. Tsoi and W. Luk. "Convex models for accelerating applications on FPGA-based clusters". In Proc. IEEE Symposium on Field-Programmable Technology (FPT), pages 495-498, 2010.
17. A.H.T. Tse, D.B. Thomas, K.H. Tsoi and W. Luk. "Reconfigurable Control Variate Monte-Carlo Designs for Pricing Exotic Options". In Proc. International Conference on Field Programmable Logic and Applications (FPL), page 364-367, 2010.
18. A.H.T. Tse, D.B. Thomas, K.H. Tsoi and W. Luk. "Efficient Reconfigurable Design for Pricing Asian Options". In Proc. International Workshop on Highly Efficient Accelerators and Reconfigurable Technologies (HEART), pages 14-20, 2010.
19. K.H. Tsoi, A.H.T. Tse, P. Pietzuch and W. Luk. "Programming Framework for Clusters with Heterogeneous Accelerators". In Proc. International Workshop on Highly Efficient Accelerators and Reconfigurable Technologies (HEART), pages 53-59, 2010.
20. K.H. Tsoi, I. Papagiannis, M. Migliavacca, W. Luk and P. Pietzuch. "Accelerating Publish/Subscribe Matching on Reconfigurable Supercomputing Platform". Many-Core and Reconfigurable Supercomputing Conference, 2010.
21. V. Sriram, K.H. Tsoi, W. Luk and D. Cox. "Design-Space Exploration of Biologically-Inspired Visual Object Recognition Algorithms Using CPUs, GPUs, and FPGAs". Many-Core and Reconfigurable Supercomputing Conference, 2010.
22. K.H. Tsoi and W. Luk. "Axel: A Heterogeneous Cluster with FPGAs and GPUs". In Proc. Field Programmable Gate Arrays (FPGA), pages 115-124, 2010.
23. O. Mencer, K.H. Tsoi, S. Cramer, T. Todman, W. Luk, M.Y. Wong and P.H.W. Leong. "Cube: A 512-FPGA cluster". In Proc. Southern Conference on Programmable Logic (SPL), pages 51-57, 2009.

24. K.H. Tsoi, D. Rueckert, C.H. Ho and W. Luk. "Reconfigurable Acceleration of 3D Image Registration". In Proc. Southern Conference on Programmable Logic (SPL), pages 95-100, 2009. **(best paper award)**
25. J.H.C. Yeung, C.C. Tsang, K.H. Tsoi, B.S.H. Kwan, C.C.C. Cheung, A.P.C. Chan and P.H.W. Leong. "Map-reduce as a programming model for custom computing machines". In Proc. IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), pages 149-159, 2008.
26. M.X. Ouyang, L.Y. Sin, K.H. Tsoi, C.T. Chow, M.K. Wong, W.J. Li, P.H.W. Leong and K.W. Wong. "Constant-power operation of functionalized carbon nanotube sensors for alcohol vapor detection". In Proc. IEEE International Conference on Nano/Micro Engineered and Molecular Systems (NEMS), pages 747-752, Jan 2008.
27. K.H. Tsoi and P.H.W. Leong. "Mullet - a parallel multiplier generator". In Proc. International Conference on Field Programmable Logic and Applications (FPL), pages 691-694, 2005.
28. G.L. Zhang, P.H.W. Leong, C.H. Ho, K.H. Tsoi, C.C.C. Cheung, D-U. Lee, R.C.C. Cheung, and W. Luk. "Reconfigurable acceleration for Monte Carlo based financial simulation". In Proc. International Conference on Field Programmable Technology (FPT), pages 215-222, 2005.
29. P.H.W. Leong and K.H. Tsoi. "Field programmable array technology for robotics applications". In Proc. IEEE International Conference on Robotics and Biomimetics (ROBIO), pages 295-298, July 2005.
30. R. Ludewig, O. Soffke, P. Zipf, M. Glesner, K.P. Pun, K.H. Tsoi, K.H. Lee and P.H.W. Leong. "IP Generation for an FPGA-based Audio DAC Sigma-Delta Converter". In Proc. International Conference on Field Programmable Logic and Applications (FPL), volume 3203 of LNCS, pages 526-535, 2004.
31. K.H. Tsoi, C.H. Ho, H.C. Yeung and P.H.W. Leong. "An arithmetic library and its application to the N-body problem". In Proc. IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), pages 68-78, 2004.
32. C.C. Cheung, K.P. Pun, C.L. Yuen, K.H. Tsoi and P.H.W. Leong. "An FPGA-based re-configurable 24-bit 96khz sigma-delta audio DAC". In Proc. International Conference on Field Programmable Technology (FPT), pages 110-117, 2003.
33. C.H. Ho, K.H. Tsoi, H.C. Yeung, Y.M. Lam, P.H.W. Leong, K.H. Lee, R. Ludewig, P. Zipf, A.G. Ortiz and M. Glesner. "Arbitrary function approximation in HDLs with application to the N-body problem". In Proc. International Conference on Field Programmable Technology (FPT), pages 84-91, 2003.
34. K.H. Tsoi, K.H. Lee and P.H.W. Leong. "Compact FPGA-based true and pseudo random number generators". In Proc. IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), pages 51-61, 2003.
35. C.H. Ho, P.H.W. Leong, K.H. Lee, K.H. Tsoi, R. Ludewig, P. Zipf, A.G. Ortiz and M. Glesner. "Fly a modifiable hardware compiler". In Proc. International Conference on Field Programmable Logic and Applications (FPL), pages 381-390, 2002.
36. K.H. Tsoi, K.H. Lee and P.H.W. Leong. "A massively parallel rc4 key search engine". In Proc. IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), pages 13-21, 2002.
37. O.Y.H. Cheung, K.H. Tsoi, P.H.W. Leong and M.P. Leong. "Tradeoffs in parallel and serial implementations of the international data encryption algorithm IDEA". In Proc. International Workshop on Cryptographic Hardware and Embedded Systems (CHES), pages 333-347, 2001.
38. M.P. Leong, O.Y.H. Cheung, K.H. Tsoi and P.H.W. Leong. "A bit-serial implementation of the international data encryption algorithm IDEA". In Proc. IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), pages 122-131, 2000.

Work Experience

Imperial College London

Research Associate
Research Manager

- Development of a sophisticated networking system for an FPGA cluster. Tasks include designing advanced routing features in the wired network for data communication and building a wireless sensor network in the 2.4GHz band for cluster monitoring and coordination. Porting applications for physical simulation and complex event processing to the Maxeler FPGA accelerator platform. Development of a medical robotic control system for surgery applications. Tasks include modeling, realization, optimization and integration of a GPU accelerator to enable quick response time during minimally invasive surgery. Research to improve the power and energy efficiency of various processing devices including CPUs, GPUs and FPGAs. (2011)
- Development of customized communication between multiple FPGAs. Tasks include building GTP based wired low latency network, porting applications utilizing the networks, accelerating Physical, biomedical and financial applications using the Alpha-Data acceleration cards. Research in GPU performance analysis and modeling with systematic optimization methods. (2010)

United Kingdom

Jan 2008 – Oct 2010
Oct 2010 – present

- Development of a high performance computing (HPC) cluster based on FPGA and GPU accelerators. Tasks include system integration, workload distribution and balancing, multi-accelerator collaboration and software framework for application development. Development of FPGA accelerated Medical Image Registration (MIR) system. Tasks include exploring trade-offs between accuracy, resource and performance, customized cache system. (2009)
- Development of a 512-FPGA cluster. Tasks include system architecture design, PCB design and layout, electronic level testing and debugging, RTL coding for FPGA design, system interfacing, work flow integration and application benchmarking. (2008)

Kontel-Data System

Engineer

Involved in multiple projects including ASIC layout of SoC designs, digital interface for analog sensors, testing and benchmarking a 12-bit ADC design and MEMS sensors, development of 5KHz ultra-low power VLF transceivers.

Hong Kong

Sep – Nov 2007

The Chinese University of Hong Kong

Research Assistant

Development of portable equipment for in-house developed Carbon Nano Tube (CNT) sensors using a microcontroller (TI MSP430). Tasks included hardware construction of an adaptive instrument for constant power measurement in micro-amp range and the supporting software.

Hong Kong

Oct 2006 – Aug 2007

Hong Kong Applied Science and Technology Research Institute Company Limited (ASTRI) Hong Kong

Member of Professional Staff

Member of Integrated Circuit Design group Mobile Terminal and Multimedia (MTM) team. This work involved the development of an H.264 co-processor prototype in an FPGA. Major duties included floating point unit design and verification, prototype board design, AMBA system development, FPGA interface and peripheral integration, LCD/DVI display unit and FPGA based H.264 optimization.

Sep 2005 – Aug 2006

Civil Service Bureau, HK Government

Contract Programmer

Developed an inter-department database system using FoxPro.

Hong Kong

May – June 2000

The Chinese University of Hong Kong

Research Assistant

DSP (TI TMS320) programming and data analysis.

Hong Kong

May - June 1998

Teaching Experience

Imperial College London

Project Supervisor

Supervising full-time PhD, MSc and undergraduate students (in Undergraduate Research Opportunities Program) in research oriented projects.

United Kingdom

July 2009 - present

Imperial College London

Teaching Assistant and Course Support Leader

Leading course support for undergraduate courses. Duties included supporting tutorial sections, helping students with exercises, marking coursework and coordinating course tutors. Courses included Computer Systems (113) and Computer Architecture (210).

United Kingdom

Jan 2008 - present

The Chinese University of Hong Kong

Teaching Assistant

Teaching assistant for both undergraduate and postgraduate courses. Duties included giving tutorial lessons, shared responsibility for exams, assignments and grading. Courses included CSC3250 Computers and Society; CSC4160 Distributed and Parallel Computing; CEG3470 Digital Circuits; CEG5010 Reconfigurable Computing.

Hong Kong

Aug 2000 - Aug 2005

Referees

<p>Dr. Wayne Luk Professor Department of Computing, Imperial College London. Email: wlu@doc.ic.ac.uk</p>	<p>Dr. Oskar Mencer CEO and CTO Maxeler Technologies London, UK Email: mencer@maxeler.com</p>	<p>Dr. Philip Leong Associate Professor School of Electrical and Information Engineering, University of Sydney. Email: phwl@ee.usyd.edu.au</p>
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