The duration of this examination is 50 minutes

Please answer *all three* questions

This examination is partly based on the Intel Core microarchitecture ("Woodcrest"), as described in the article "Intel's Next Generation Microarchitecture Unveiled" (David Kanter, Real World Technologies, 9 March 2006), which you should have available to you in the examination. Where the article is incomplete, you are invited to speculate using your understanding of the underlying architectural principles.

1 The Woodcrest microarchitecture includes an Internal Results Bus (IRB), which supports up to four completing instructions per cycle. Identify *three* conceptual elements of the microarchitecture which need to monitor the Internal Results Bus. For each of the three cases, explain carefully how the result data is eventually used (not all the IRB destinations are shown in the block diagram in the article).

2 Consider the following loop nest, which produces the transpose of a matrix of 8-byte doubles:

```
for (i=0; i<N; i++) {
   for (j=0; j<N; j++) {
     B[i][j] = A[j][i];
   }
}
```

a Estimate the value of `N` above which all accesses to `A` will be misses in Woodcrest's L1 data cache. Assume, the sake of this question, that no prefetching occurs, and there are no associativity conflicts.

b Suppose N is actually large. Show how this loop nest could be restructured so that the L1 data cache is used effectively.

The two parts carry equal marks.

3 a How is Woodcrest's Indirect Branch Predictor indexed?

b In ideal circumstances, a taken branch can be executed without a stall. In the worst case, the cost of a branch could be a full misprediction penalty. Explain how the cost of an individual branch might lie somewhere between these extremes.

c It has been suggested that the two cores should share a common branch predictor. Identify, and explain, several advantages and several disadvantages of this idea.

The three parts carry, respectively, 25%, 25%, and 50% of the marks.