

QIANG LIU

9, Linden Avenue, London, NW10 5QY, U.K.

Mobile: +44(0)7725882099 • qiang.liu2@imperial.ac.uk

HIGHLIGHTS

- Research Associate currently in Department of Computing at Imperial College London
- PhD degree in digital system design in Electrical and Electronic Engineering Department at Imperial College London
- Research interests in high performance reconfigurable computing system design, including system architecture, code transformation, design automation and optimization techniques, and high speed and low power applications
- Awarded the **Eryl Cadwaladr Davies Prize** for producing the best doctoral thesis in Department of Electrical and Electronic Engineering at Imperial College London in 2009
- Runner-up in the 2009 British Computer Society Distinguished Dissertation Competition
- 15 papers published in Journals and international conferences
- 1.5 year work experience in STMicroelectronics Co. Ltd

WORK EXPERIENCE

Computing Department of Imperial College London, London, U.K.

2009 - present

Research Associate

- Develop source code-level optimization tools for C-level reconfigurable system design
- Focus on mathematical model-based design space exploration and transformations
- Develop static and run-time optimization techniques targeting high speed and low power reconfigurable computing systems, for signal processing, scientific computation and finance analysis
- Tutor undergraduates for courses on Networks and Communications, and Computer Architecture

STMicroelectronics Co. Ltd, Beijing, China

2004 - 2005

Software Development and Application Engineer

- Designed digital TV solutions based on Chinese market and developed Linux low level drivers
- Worked on site to identify and solve problems encountered by clients and provided training to clients

EDUCATION

Imperial College, London, U.K.

2005 - 2008

PhD in Electrical and Electronic Engineering

- Title: Data Reuse and Parallelism in Hardware Compilation
- Proposed a 4-step systematic approach to optimize data storage and transfer, and customise parallel data path in reconfigurable system design to achieve the best trade-off between power consumption, performance and hardware resources
- Formulated and solved optimization problems leveraging linear, nonlinear, parametric integer programming and geometric programming theories

Tianjin University, Tianjin, China

2001 - 2004

Master of Science in Electrical and Electronic Engineering

- Top 1 in class, GPA 3.7/4.0
- Title: New Generation HDTV Set-Top Box

Tianjin University, Tianjin, China

1997 - 2001

Bachelor of Science in Electrical and Electronic Engineering

- Ranked the 9th in 150 students, GPA 3.6/4.0

AWARDS

- 2009 Eryl Cadwaladr Davies Prize for producing the best doctoral thesis in Department of Electrical and Electronic Engineering at Imperial College London in 2009
- 2009 Runner-up in the 2009 CPHC/BCS Distinguished Dissertation Competition
- 2005-2008 Scholarship of Department of EEE, Imperial College, £28k/year
- 1997-2002 Huawei Award of ¥2.5k, and 4 times Three-Good Student of Tianjin University, awarded to student who distinguished himself in each academic year

SELECTED PUBLICATIONS

Journal:

- [1]. Q. Liu, Tim Todman, Wayne Luk and G. A. Constantinides. "Optimizing Hardware Design by Composing Utility-Directed Transformations". Minor correction to *IEEE Transaction on Computers*, July, 2011.
- [2]. Q. Liu, Tim Todman, Wayne Luk and G. A. Constantinides. "Automated Mapping of the MapReduce Pattern Onto Parallel Computing Platforms". In *Journal of Signal Processing Systems*, Dec., 2010.
- [3]. Q. Liu, G. A. Constantinides, K. Masselos and P. Y. K. Cheung. "Combining data reuse exploitation with data-level parallelization for FPGA targeted hardware compilation: a geometric programming framework". In *IEEE Transaction on CAD*, volume 28, number 3, pp. 305-315, March, 2009.
- [4]. Q. Liu, G. A. Constantinides, K. Masselos and P. Y. K. Cheung. "Data reuse exploration under an on-chip memory constraint for low power FPGA-based systems". In *IET Computers and Digital Techniques*, October, 2008.
- [5]. Q. Liu, G. A. Constantinides, K. Masselos and P. Y. K. Cheung. "Compiling C-like Languages to FPGA Hardware: Some Novel Approaches Targeting Data Memory Organisation". In *The Computer Journal*, volume 52, issue 2, pp. 1-10, March, 2009.

Conference:

- [1]. Q. Liu, T. Mak, J. Luo, W. Luk and A. Yakovlev. "Power Adaptive Computing System Design in Energy Harvesting Environment". In International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, Samos, Greece, July, 2011
- [2]. Tim Todman, Q. Liu, Wayne Luk and G. A. Constantinides. " Customizable Composition and Parameterization of Hardware Design Transformations". In *13th Euromicro conference on Digital System Design*, Lille, France, September, 2010.
- [3]. Q. Liu, Tim Todman, and Wayne Luk. "Combining Optimizations in Automated Low Power Design". In *International Conference on Design, Automation & Test in Europe*, Germany, March, 2010.
- [4]. Q. Liu, Tim Todman, Wayne Luk and G. A. Constantinides. "Automatic Optimisation of Map-Reduce Designs by Geometric Programming". In *IEEE International Conference on Field Programmable Technology*, Sydney, Australia, December, 2009.
- [5]. Q. Liu, Tim Todman, Jose Gabriel de F. Coutinho, Wayne Luk and G. A. Constantinides. "Optimising Designs by Combining Model-Based and Pattern-Based Transformations". In *IEEE International Conference on Field Programmable Logic and Applications*, Prague, Czech, Sept., 2009.
- [6]. Q. Liu, G. A. Constantinides, K. Masselos and P. Y. K. Cheung. "Combining Data Reuse Exploitation with Data-Level Parallelization for FPGA Targeted Hardware Compilation: A Geometric Programming Framework". In *18th IEEE Int. Conf. on FPL*, pp. 179-184, Germany, September, 2008.
- [7]. Q. Liu, G. A. Constantinides, K. Masselos and P. Y. K. Cheung. "Automatic On-Chip Memory Minimization for Data Reuse". In *15th IEEE Symposium on FCCM*, pp.251-260, USA, April, 2007.
- [8]. Q. Liu, K. Masselos and G. A. Constantinides. "Data reuse exploration for FPGA based platforms applied to the full search motion estimation algorithm". In *Proc. 16th IEEE International Conference on Field Programmable Logic and Applications*, Madrid, Spain, August, 2006.