Compilers - Chapter 6: Optimisation and data-flow analysis **Part 1: Introduction to optimisation**

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- Materials:
 - materials.doc.ic.ac.uk, Panopto
 - Textbook
 - Course web pages

(http://www.doc.ic.ac.uk/~phjk/Compilers)

– Piazza

(https://piazza.com/class/kf7uelkyxk7aa)

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Overview

- This introductory course has focussed so far on fast, simple techniques which generated code that works reasonably well
- We now briefly look at what *optimising* compilers do, and how they do it
- Compare "gcc file.c" versus "gcc –O file.c"
- According to the gcc manual page ("man gcc"):
 - Without `-O', the compiler's goal is to reduce the cost of compilation and to make debugging produce the expected results. Statements are independent: if you stop the program with a breakpoint between statements, you can then assign a new value to any variable or change the program counter to any other statement in the function and get exactly the results you would expect from the source code.
 - Without `-O', only variables declared "register" are allocated in registers

The plan

- To optimise or not to optimise?
- High-level vs low-level; role of analysis
- Peephole optimisation
- Local, global, interprocedural
 - Loop optimisations
 - Where optimisation fits in the compiler
 - Example: live ranges
 - -Live ranges as a data flow problem
 - -Solving the data-flow equations
 - -Deriving the interference graph
 - Other data-flow analyses
 - Next chapter • Loop-invariant code and code motion op. isations
 - More sophisticated optimisations

This chapter

Optimisation: example

• Consider the loop from tutorial exercise 4:

```
void P(int i, int j)
 int k, tmp;
 for (k=0; k<100; k++) {
  tmp = A[i+k];
  A[i+k] = A[j+k];
  A[j+k] = tmp;
```

• What can optimisation do here?

Without optimisation.... _P: subl \$36,%esp pushl %ebp pushl %ebx nop movl \$0,28(%esp) .align 4 L3: cmpl \$99,28(%esp) ile L6 jmp L4 .align 4 L6: movl 48(%esp),%eax movl 28(%esp),%edx addl %edx,%eax leal 0(,%eax,4),%edxmovl \$_A,%eax movl (%edx,%eax),%edx movl %edx,24(%esp) movl 48(%esp),%eax movl 28(%esp),%ecx leal (%ecx,%eax),%edx leal 0(.%edx,4).%eax

movl \$_A,%edx movl 52(%esp),%ecx movl 28(%esp),%ebx addl %ebx,%ecx leal 0(,%ecx,4),%ebxmovl \$_A,%ecx movl (%ebx,%ecx),%ebx movl %ebx,(%eax,%edx) movl 52(%esp),%eax movl 28(%esp),%ecx leal (%ecx,%eax),%edx leal 0(,%edx,4),%eaxmovl \$_A,%edx movl 24(%esp),%ecx movl %ecx,(%eax,%edx) L5: incl 28(%esp)

jmp L3 .align 4 L4: L2: popl %ebx popl %ebp addl \$36,%esp ret Without optimisation, code is large, slow, but compiles quickly and works well with the debugger

31 instructions in loop Performance:

• 8.2ns per iteration (gcc 3.2.2, 2GHz Pentium IV)

With optimisation:

- In this extreme example, optimised code is 2-4 times faster
 - Use registers not stack
 - One jump per iteration
 - Loop-invariant offset calculation moved out
 - Array pointers incremented instead of recalculated
 - Loop control variable replaced with down-counter

```
_P: pushl %edi
pushl %esi
movl $99,%edi
pushl %ebx
movl $_A,%esi
movl $_A,%esi
movl 20(%esp),%ebx
movl 16(%esp),%ecx
sall $2,%ebx
sall $2,%ecx
.align 4
```

```
L6:
```

```
movl (%esi,%ecx),%edx
movl (%esi,%ebx),%eax
movl %eax,(%esi,%ecx)
movl %edx,(%esi,%ebx)
addl $4,%ecx
             8 instructions in loop
addl $4,%ebx
decl %edi
             Performance:
jns L6
                3.4ns per iteration
popl %ebx
popl %esi
                (gcc 3.2.2, 2GHz
popl %edi
                Pentium IV)
ret
```

With optimisation:

- In this extreme example, optimised code is 2-4 times faster
 - Use registers not stack
 - One jump per iteration
 - Loop-invariant offset calculation moved out
 - Array pointers incremented instead of recalculated
 - Loop control variable replaced with down-counter

_P:	pushl %es	İ
	pushl %eb	K
	movl 12(%	esp), %edx
	movl 16(%	esp), %ecx
	leal 0(,%e	dx,4), %ebx
	subl %edx	, %ecx
	movl %ecx	k, %edx
	leal _A(%e	ebx), %eax
	addl \$_A+	400, %ebx
L2:	movl (%ea	ix), %ecx
	movl (%ea	ix,%edx,4), %esi
	movl %esi	, (%eax)
	movl %ecx	<, (%eax,%edx,4)
	addl \$4, %	eax
	cmpl %eb	x, %eax
	jne L2	7 instructions in loss
	popl %ebx	7 instructions in loop
	popl %esi	• 0.7ns per iteration
	ret	(gcc 5.4 –O3,
		3.2GHz Intel

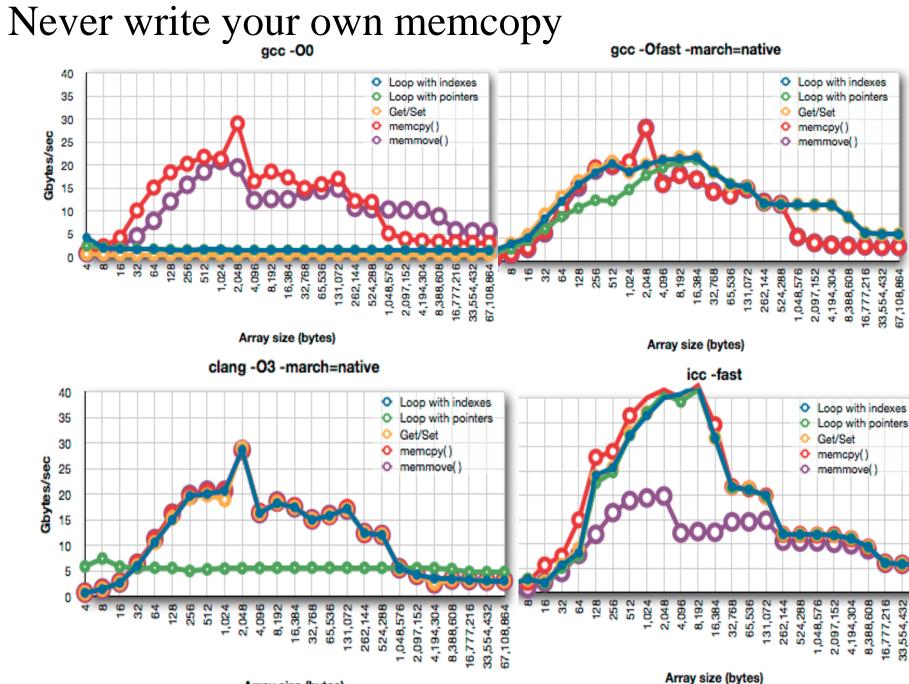
Skylake i76600U)

With optimisation:

_P:

- In this code, the compiler has used vector instructions that operate on four operands at a time
- The full code is rather complicated as care is needed to check whether the memory regions overlap
- (this example goes far beyond what we can hope to cover in this course)

.L5: movdqu (%rdx,%rax), %xmm0 movdqu (%rcx,%rax), %xmm1 movdqu %xmm1, (%rdx,%rax) movdqu %xmm0, (%rcx,%rax) \$16, %rax addq \$400, %rax cmpq .L5 jne 7 instructions in loop rep ret 0.2ns per iteration (gcc 4.8.4 – O3, -march=native, **3.2GHz Intel** Skylake i7-6600U) Vectorised



Array size (bytes)

http://nadeausoftware.com/articles/2012/05/c_c_tip_how_copy_memory_quickly

67,108,864

33,554,432

67,108,864

Optimisation principles...

- To generate really good code, need to combine many techniques, including both high-level and low-level
- High-level example: inlining
 - replace a call "f(x)" with the function body itself
 - Avoids call/return overheads
 - Also creates further opportunities...
 - Can we inline virtual method calls "x.f(y)"?
 - Need *static analysis* of possible types of "x"
- Low-level example: instruction scheduling
 - Re-order instructions so processor executes them in parallel
 - To switch order of load A[i] and store A[j], need dependence analysis: could i and j refer to same location?

- A simple local technique peephole optimisation
 - Scan assembly code, replacing obviously inane combinations of instructions (eg mov R0,a; mov a,R0)
 - Easy to implement:

```
peep :: [Instruction] -> [Instruction]
peep (Store r1 dest : Load r2 src : rest)
| src == dest
= Store r1 dest : (peep (Load r2 r1 : rest))
| otherwise
```

- = Store r1 dest : (peep (Load r2 src : rest))
- Endless possibilities...
- *Phase ordering problem*: in which sequence should optimisations be applied?

Spectrum...

- Peephole optimisation works at instruction level
- The Sethi-Ullman "weights" algorithm: expressions
- "Local" optimisation works at the level of *basic blocks* a sequence of instructions which has a single point of entry and a single point of exit
- "Global" optimisation works on a whole procedure
- **Interprocedural** optimisation works on the whole program
- Local: generally runs quickly and easy to validate
- Global: may have worse-than-linear complexity, eg $O(N^2)$ where *N* is number of instructions, basic blocks, or local variables
- Interprocedural: rare hard to avoid excessive compilation time

Some loop optimisations...

- Loop-invariant code motion
 - An instruction is **loop-invariant** if its operands can only arrive from outside the loop
 - move loop-invariant instructions into loop header
- Detection of induction variables
 - Induction variable is a variable which increases/decreases by a (loop-invariant) constant on each iteration
- **Strength reduction**: calculate induction variable by incrementing, instead of by multiplying other induction variables
- **Control variable selection**: replace loop control variable with one of the induction variables actually used in the loop

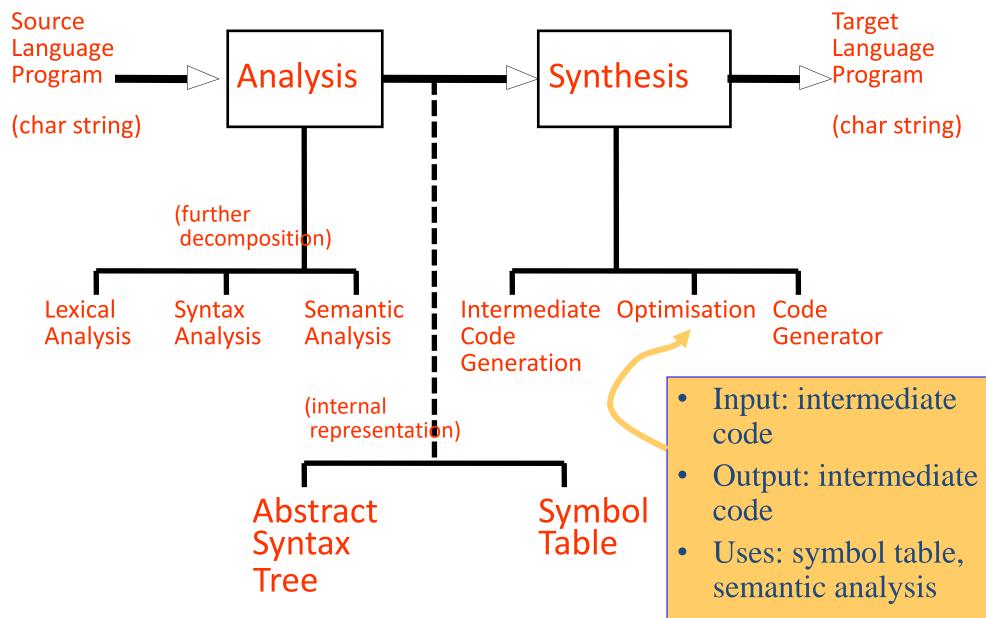
int P(int N, int M) int i, u, v, w, x, y; int z = 0; for (i=0; i<N; i++) { w = w + 10; $x = w^{*}10;$ $\underline{\mathbf{y}} = \mathbf{z}^{*}(\mathbf{w} \cdot \mathbf{x});$ u = w + x + y + N + M;v = v+u;return v;

Loop optimisations - example

- 1. y is constant
- 2. w-x is dead code
- 3. y+N+M is loopinvariant
- 4. i, w and x are induction variables (so is w+x)
- 5. x increases by 100 each iteration
- 6. i is used only to control the loop, and can be omitted if convenient

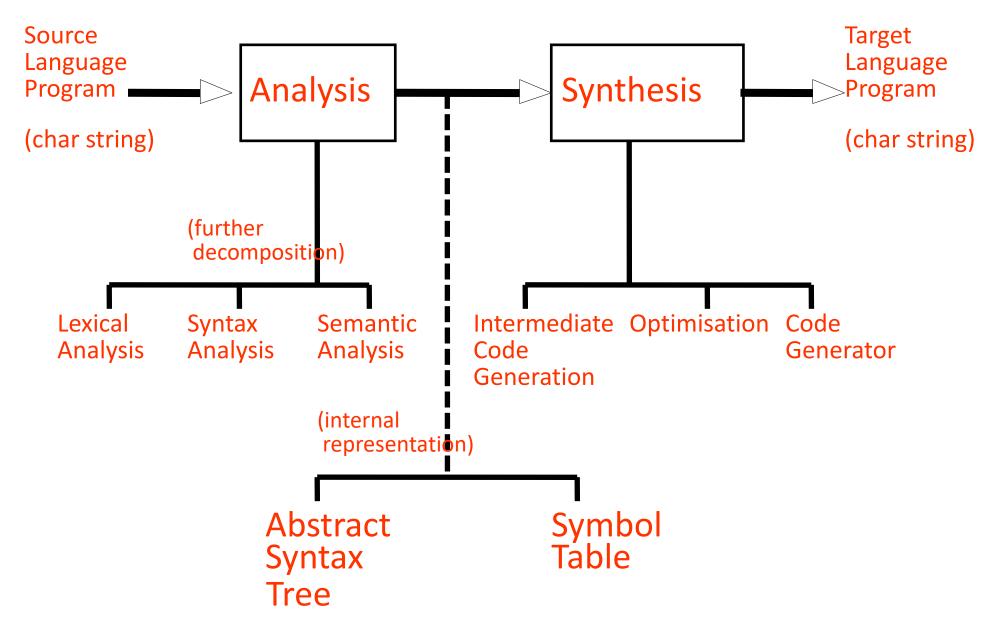
- 1. (constant propagation Appel pg457)
- 2. (dead code elimination pg457,397)
- 3. (loop-invariant code motion pg422)
- 4. (induction variable recognition pg426)
- 5. (strength reduction ditto)
- 6. (rewriting comparisons, pg428)

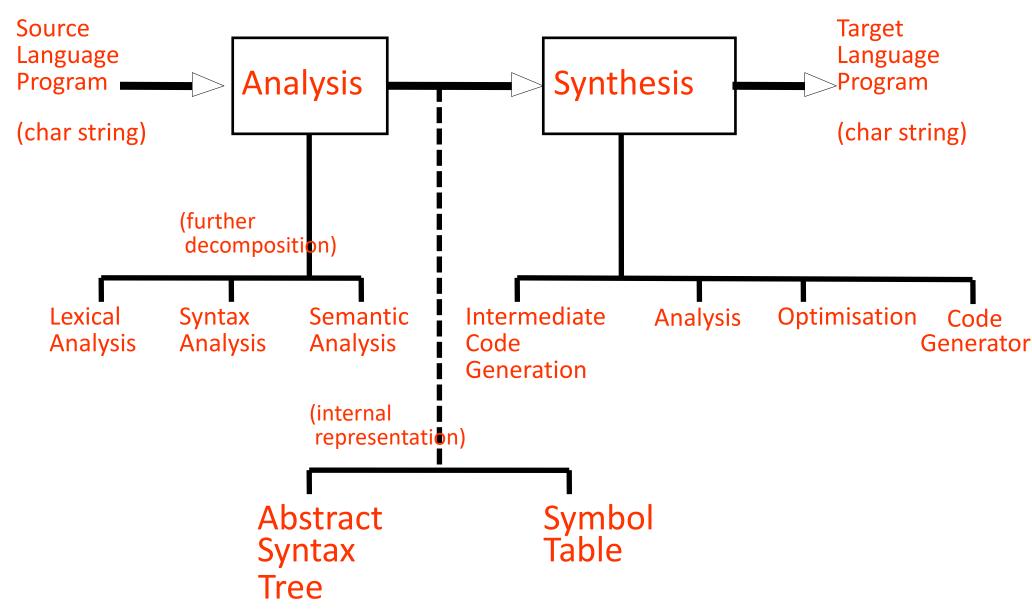
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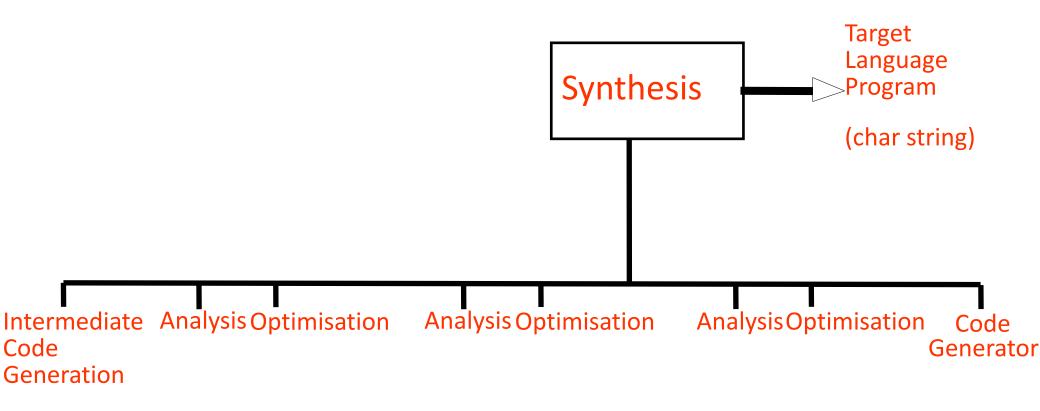


Intermediate code

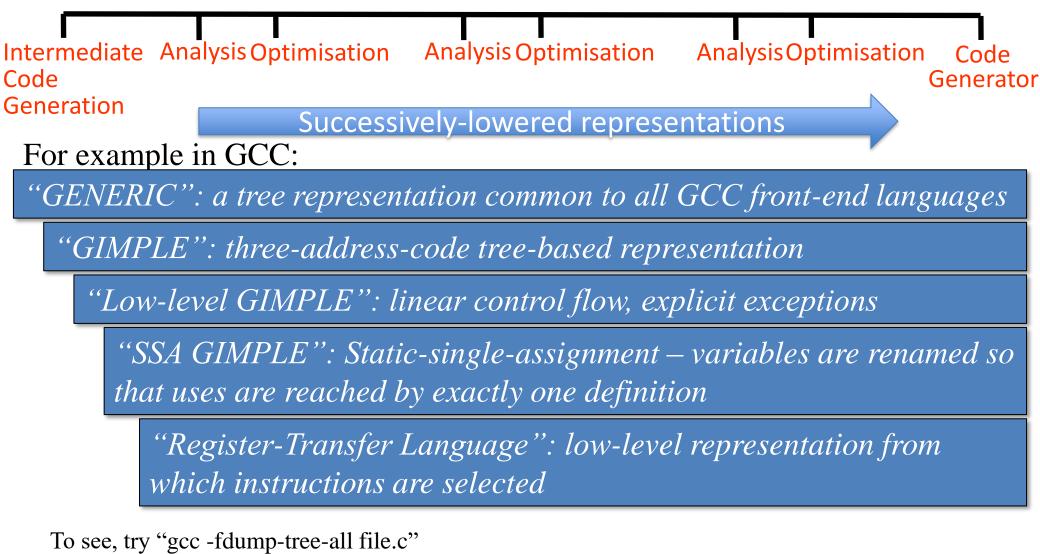
- In our simple compiler, translator traverses AST and produces assembler code directly
- In optimising compiler, translator traverses AST and produces "intermediate code"
- Intermediate code is designed to
 - Represent all primitive operations necessary to execute program
 - In a uniform way, easy to analyse and manipulate
 - Independently of target instruction set
- Compiler writers argue... Appel advocates two IRs:
 - Tree: before instruction selection
 - FlowGraph: after instruction selection
- IR uses "temporaries" T0, T1, T2... instead of real registers; after optimisation, use graph colouring to assign temporaries to real registers







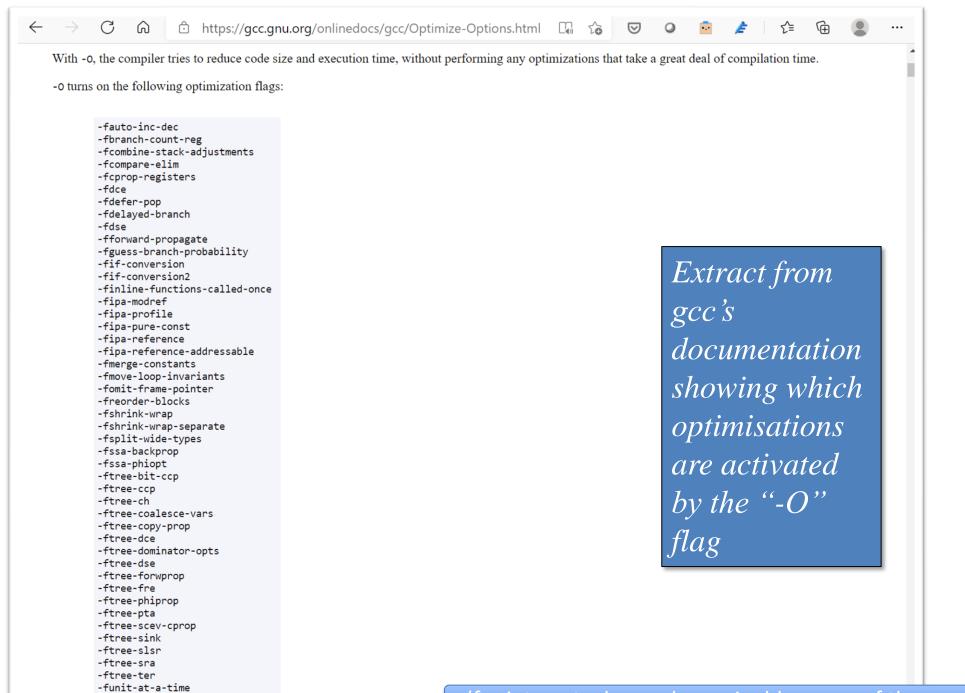




Or on Compiler Explorer:

https://godbolt.org/z/78qd4r for GIMPLE

https://godbolt.org/z/7WW4vT for RTL



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-fauto-inc-dec		LEVELS_1_PLUS, OPT_fcprop_registers, NULL, 1 },			
-fbranch-count-reg	· _	LEVELS_1_PLUS, OPT_fdefer_pop, NULL, 1 },			
-fcombine-stack-adjustments		LEVELS_1_PLUS, OPT_fforward_propagate, NULL, 1 },			
-fcompare-elim		LEVELS_1_PLUS, OPT_fguess_branch_probability, NULL, 1 },			
-fcprop-registers		LEVELS_1_PLUS, OPT_fipa_profile, NULL, 1 },			
-fdce -fdefer-pop		LEVELS_1_PLUS, OPT_fipa_pure_const, NULL, 1 },			
-fdelayed-branch		LEVELS_1_PLUS, OPT_fipa_reference, NULL, 1 },			
-fdse	· _	LEVELS_1_PLUS, OPT_fipa_reference_addressable, NULL, 1 },			
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-ftree-dce	46. #endif				
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-ftree-dse -ftree-forwprop	165 { OPT_	LEVELS_1_PLUS_NOT_DEBUG, OPT_fif_conversion, NULL, 1 },			
-ftree-fre	166 { OPT_	LEVELS_1_PLUS_NOT_DEBUG, OPT_fif_conversion2, NULL, 1 },			
-ftree-phiprop		LEVELS 1 PLUS NOT DEBUG, OPT finline functions called once, N	ULL, 1 },		
-ftree-pta		LEVELS_1_PLUS_NOT_DEBUG, OPT_fmove_loop_invariants, NULL, 1 }			
-ftree-scev-cprop		LEVELS_1_PLUS_NOT_DEBUG, OPT_fssa_phiopt, NULL, 1 },			
-ftree-sink -ftree-slsr	170 { OPT_	LEVELS_1_PLUS_NOT_DEBUG, OPT_fipa_modref, NULL, 1 },			
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With -0, the compiler tries to reduce code		<pre>s 421 NEXT_PASS (pass_instantiate_virtual_regs);</pre>
with -0, the complier tries to reduce code	430 {	422 NEXT_PASS (pass_into_cfg_
-0 turns on the following optimization fla	ac 431 /* -O1 and -Og optimizations. */	423 NEXT PASS (pass jump); Small extract from
	432 { OPT_LEVELS_1_PLUS, OPT_fcombine_stack_adjustmer	
	433 { OPT_LEVELS_1_PLUS, OPT_fcompare_elim, NULL, 1	1 424 NEXT_PASS (pass_lower_sub
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-fmerge-constants -fmove-loop-invariants	451 { OPT_LEVELS_1_PLUS, OPT_ftree_copy_prop, NULL, :	3 -
-fomit-frame-pointer	452 { OPT_LEVELS_1_PLUS, OPT_ftree_dce, NULL, 1 },	439 NEXT_PASS (pass_loop2);
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-fshrink-wrap	454 { OPT_LEVELS_1_PLUS, OPT_ftree_fre, NULL, 1 },	441 NEXI PASS (pass rtl loop init);
-fshrink-wrap-separate -fsplit-wide-types	455 { OPT_LEVELS_1_PLUS, OPT_ftree_sink, NULL, 1 },	, A42 NEXT DASS (noss stl move lean invenients);
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-fssa-phiopt	457 { OPT_LEVELS_1_PLUS, OPT_ftree_ter, NULL, 1 },	
-ftree-bit-ccp	458 459 /* -O1 (and not -Og) optimizations. */	444 NEXT_PASS (pass_rtl_doloop);
-ftree-ccp -ftree-ch	<pre>459 /* -O1 (and not -Og) optimizations. */ 460 { OPT_LEVELS_1 PLUS NOT_DEBUG, OPT_fbranch_count</pre>	445 NEXT_PASS (pass_rtl_loop_done);
-ftree-coalesce-vars	400 [OFI_LEVELS_I_FLOS_NOI_DEBOG, OFI_IDFAILIN_COUNC	446 POP_INSERT_PASSES ()
-ftree-copy-prop	<pre>{ OPT_LEVELS_1_PLUS_NOT_DEBUG, OPT_fdelayed_brand</pre>	and 447 NEXT_PASS (pass_lower_subreg2);
-ftree-dce	46 #endif	
-ftree-dominator-opts	464 { OPT_LEVELS_1_PLUS_NOT_DEBUG, OPT_fdse, NULL, 1	1 A8 NEXT_PASS (pass_web);
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-ftree-phiprop	467 { OPT_LEVELS_1_PLUS_NOT_DEBUG, OPT_finline_funct:	ct: 451 NEXT_PASS (pass_rtl_dse1);
-ftree-pta	468 { OPT_LEVELS_1_PLUS_NOT_DEBUG, OPT_fmove_loop_inv	in 452 NEXT PASS (pass rtl fwprop addr):
-ftree-scev-cprop -ftree-sink	469 { OPT_LEVELS_1_PLUS_NOT_DEBUG, OPT_fssa_phiopt, 1	, MEVE DASS (mass ins doc):
-ftree-slsr	470 { OPT_LEVELS_1_PLUS_NOT_DEBUG, OPT_fipa_modref, I	, 1
-ftree-sra	471 { OPT_LEVELS_1_PLUS_NOT_DEBUG, OPT_ftree_bit_ccp,	
-ftree-ter	472 { OPT_LEVELS_1_PLUS_NOT_DEBUG, OPT_ftree_dse, NUI	455 NEXT_PASS (pass_ud_rtl_dce);
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Summary

- Optimisations consist of analyses and transformations
- Key optimisations include common sub-expression elimination, loopinvariant code motion, induction variable selection, strength reduction, dead code elimination (there are many more)
- Low-level optimisations: instruction selection, instruction scheduling, register allocation
- High-level optimisations: function inlining, loop unrolling often *enable* other optimisations
 - The *phase ordering problem* is the challenge of finding the right order in which to apply optimisations
- *Intermediate representations* (IRs) are designed to make analyses and optimisations easy
- Compilers successively *lower* high-level IR to low-level IR
- Optimisation algorithms that work at the function level may have worsethan-linear time complexity
 - But inter-procedural, whole-program ("link time") optimisations need to be O(n)

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1			A • • ○	utput 👻 🍸 F	ilter 👻 🖪 Libraries	+ Add new 👻 🖌 Add tool 👻			(int i, int j)			
2	int A[1000];		1	P(int	, int):			2 {	int k;			
3			2		movsx	rcx, edi	- 22		<pre>int tmp;</pre>			, and the second second
4	void P(int i, int j)		3		lea	rdi, [0+rcx*4]		5	# DEBUG BEGIN STMT			
5	{		4		lea	rax, A[rdi]			# DEBUG BEGIN_STMT			
6	int k, tmp;		5		add	rdi, OFFSET FLAT: <u>A</u> +400		8	k = 0; <d.2336>:</d.2336>			
7			6		movsx	rdx, esi			# DEBUG BEGIN_STMT			
8	for (k=0; k<100; k++)	{	7		sub	rdx, rcx		11 12	<pre>if (k > 99) goto <[<d.2337>:</d.2337></pre>	J.2334>; else	goto <0.233/>	;
9	<pre>tmp = A[i+k];</pre>	-	8	.L2:		,			<pre># DEBUG BEGIN_STMT _1 = i + k;</pre>			
10	A[i+k] = A[j+k];		9		mov	ecx, DWORD PTR [rax]			1 - 1 + K; tmp = A[_1];			
10	A[j+k] = tmp;		10		mov	esi, DWORD PTR [rax+rdx*4]			<pre># DEBUG BEGIN_STMT _2 = j + k;</pre>			
12	}		11		mov	DWORD PTR [rax], esi			_3 = i + k;			
13	ر ۲		12		mov	DWORD PTR [rax+rdx*4], ecx	,	19 20	_4 = A[_2]; A[_3] = _4;			
14	J		13		add	rax, 4		21	<pre># DEBUG BEGIN_STMT</pre>			
14			14		cmp	rax, rdi			_5 = j + k; A[_5] = tmp;			
			15		jne	<u>.L2</u>		24	# DEBUG BEGIN_STMT			
			16		ret	• • • • • • • • • • • • • • • • • • • •		25 26	<pre>k = k + 1; goto <d.2336>;</d.2336></pre>			
			17	۸.	Tet			27	<d.2334>:</d.2334>			
				A:		4000		28 } 29				
			18		.zero	4000		30				
								31				
				out (0/0) x86-64	4 gcc 10.2 🧯 - 828ms (6819B							
					. gee . o.c		0.7		C1 11			

To see GCC's intermediate representations for yourself, try "gcc -fdump-tree-all file.c" Or on Compiler Explorer: <u>https://godbolt.org/z/78qd4r</u> for GIMPLE (shown above) <u>https://godbolt.org/z/7WW4vT</u> for RTL (next slide)

$\leftarrow \ \ \rightarrow$	C ⋒						126 🖾 🤷 💿 🖉 🚖 🕼 📳 …
	APILER Add More			Ge	t cool gear in the Compiler Explorer shop ×		Sponsors intel PC-lint State Other Policies
C++ source #1	×		-	(Editor #1, Compiler #1) C++ X			5
	•• v β π C++	-		i4 gcc 10.2 🔻 🔮 -O		*	A 236r.expand Passes Options
1					es	TI	<pre>1 2 ;; Function P (_Z1Pii, funcdef_no=0, decl_uid=2330, cgraph_uid=1, symbo 3</pre>
	int A[1000];			P(int, int):		1000	4
3			2	movsx	•		5 ;; Generating RTL for gimple basic block 2
	void P(int i, int j)		3	lea	rdi, [0+rcx*4]		7 ;; Generating RTL for gimple basic block 3
	{		4	lea	rax, A[rdi]		9 ;; Generating RTL for gimple basic block 4
6	int k, tmp;		5	add	rdi, OFFSET FLAT: <u>A</u> +40		8 9 ;; Generating RTL for gimple basic block 4 10 11 12 try_optimize_cfg iteration 1 13
7			6	movsx	•		14 Merging block 3 into block 2
8	for (k=0; k<100; k++) {		7	sub	rdx, rcx		15 Merged blocks 2 and 3. 16 Merged 2 and 3 without moving.
9	tmp = A[i+k];			.L2:			17 Forwarding edge 4->5 to 6 failed. 18 Merging block 6 into block 5
10	A[i+k] = A[j+k];		9	mov	ecx, DWORD PTR [rax]		19 Merged blocks 5 and 6. 20 Merged 5 and 6 without moving.
11	A[j+k] = tmp;		10	mov	esi, DWORD PTR [rax+r		21 22
12	}		11	mov	DWORD PTR [rax], esi		23 try_optimize_cfg iteration 2
13	}		12	mov	DWORD PTR [rax+rdx*4]		25 26
14			13	add	rax, 4		<pre>27 ;; 28 ;; Full RTL generated for this function:</pre>
			14	cmp	rax, rdi		29 ;; 30 (note 1 0 5 NOTE_INSN_DELETED)
			15	jne	<u>.L2</u>		<pre>31 (note 5 1 2 2 [bb 2] NOTE_INSN_BASIC_BLOCK) 32 (insn 2 5 3 2 (set (reg/v:SI 94 [i])</pre>
			16	ret			<pre>33 (reg:SI 5 di [i])) "./example.cpp":5:1 -1 34 (nil))</pre>
			17	A:			35 (insn 3 2 4 2 (set (reg/v:SI 95 [j]) 36 (reg:SI 4 si [j])) "./example.cpp":5:1 -1
			18	.zero	4000		37 (nil)) 38 (note 4 3 7 2 NOTE_INSN_FUNCTION_BEG)
							39 (debug_insn 7 4 8 2 (debug_marker) "./example.cpp":6:3 -1 40 (nil))
							41 (debug_insn 8 7 9 2 (debug_marker) "./example.cpp":8:3 -1 42 (nil))
							<pre>43 (debug_insn 9 8 10 2 (var_location:SI k (const_int 0 [0])) -1 44 (nil))</pre>
							45 (debug_insn 10 9 11 2 (debug_marker) "./example.cpp":8:14 -1 46 (nil))
							47 (insn 11 10 12 2 (set (reg:DI 85 [_18]) 48 (sign_extend:DI (reg/v:SI 94 [i]))) -1
							49 (nil)) 50 (insn 12 11 13 2 (parallel [
							51 (set (reg:DI 86 [_19]) 52 (ashift:DI (reg:DI 85 [_18])
							53 (const_int 2 [0x2])) 54 (clobber (reg:CC 17 flags))
							55]) -1 56 (nil))
							57 (insn 13 12 14 2 (parallel [58 (set (reg:DI 83 [ivtmp.9])
							59 (plus:DI (reg:DI 86 [_19])
			C 🗒 Outpur	t (0/0) x86-64 gcc 10.2 i - 973ms (58198)		60 (symbol_ref:DI ("A") [flags 0x2] <var_decl 0x7ff2c<="" td=""> 61 (clobber (reg:CC 17 flags))</var_decl>

Feeding curiosity

- The idea of automatically deriving the instruction selector from the definition of the instruction set dates back to a landmark paper by Susan Graham and Stephen Glanville, "A new method for compiler code generation" (POPL78, https://dl.acm.org/doi/10.1145/512760.512785). The algorithm works as a bottom-up (shift-reduce) parser using the table contruction ideas you have learned about.
- There is a wonderful book "20 Years of the ACM SIGPLAN Conference on Programming Language Design and Implementation 1979-1999, A Selection" full of good things (<u>https://dblp.org/db/conf/pldi/pldi2004best.html</u>) including:
 - "Automatic generation of peephole optimizations" (Davidson and Fraser, <u>https://dl.acm.org/doi/10.1145/989393.989407</u>): peephole optimisers don't have to be ad-hoc. You can use the automatic instruction selection mechanism to translate instruction sequences *back* to IR, and *regenerate* them – and then use this to generate peephole optimisation rules. See also Souper (<u>https://github.com/google/souper</u>).
 - If you've formalised the ISA, you should be able to *prove* the correctness of peephole optimisations see "Provably correct peephole optimizations with ALIVE" (Nuno Lopes et al, PLDI'15, <u>https://dl.acm.org/doi/10.1145/2737924.2737965</u>)
 - "Global register allocation at link time" (David Wall, <u>https://dl.acm.org/doi/10.1145/989393.989415</u>). Instead of having a fixed ABI to determine which registers can be used in each function, look at the whole program to find all the call sites.