

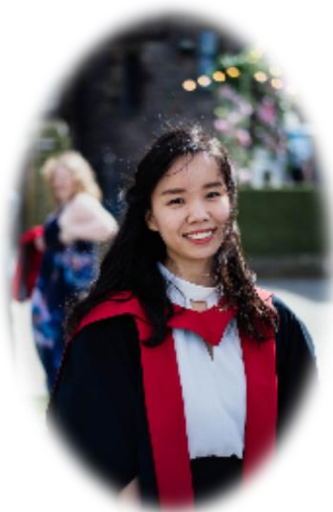
Beyond Status-Quo NPUs: Hardware-Native Multi-Tenancy & Adaptive Inference

Stylianos I. Venieris

- Sept 10th 2024
 - Samsung AI Center, Cambridge, UK
- 



Stylianos (Stelios) Venieris



Rui Li



Alexandros Kouris



Hongxiang Fan



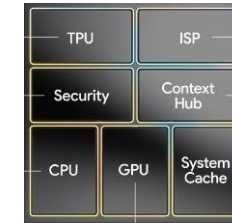
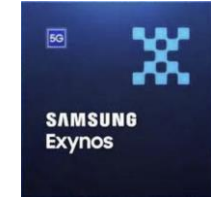
Konstantin Mishchenko



Hao (Mark) Chen

The Power of Neural Processing Units (NPUs)

- Becoming ubiquitous across mobile devices, robots and cloud servers
- Backbone of deployed AI, enabling everything from facial recognition to advanced chatbots



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Existing NPUs are optimised for:

- CNNs | Single-DNN execution

New Challenges

- 1 New DNN architectures (Transformers, Diffusion)
- 2 Multi-tenancy (multi-DNN workloads)
- 3 Diverse KPIs (latency, throughput, accuracy)



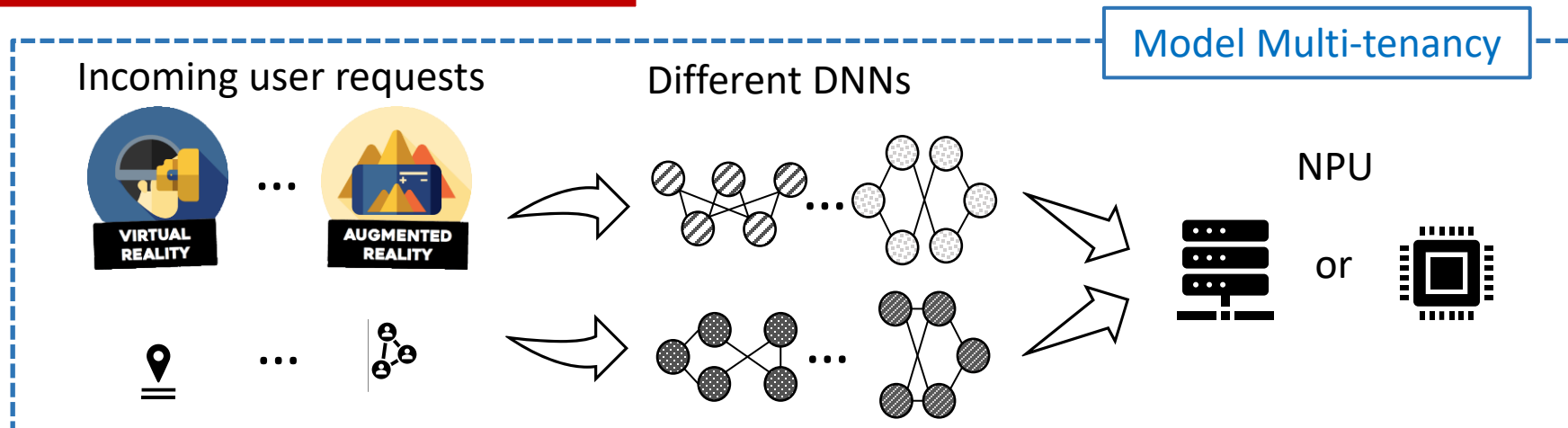
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A New Class of NPUs: Multi-DNN Accelerators

- NPUs with native support for multi-model execution

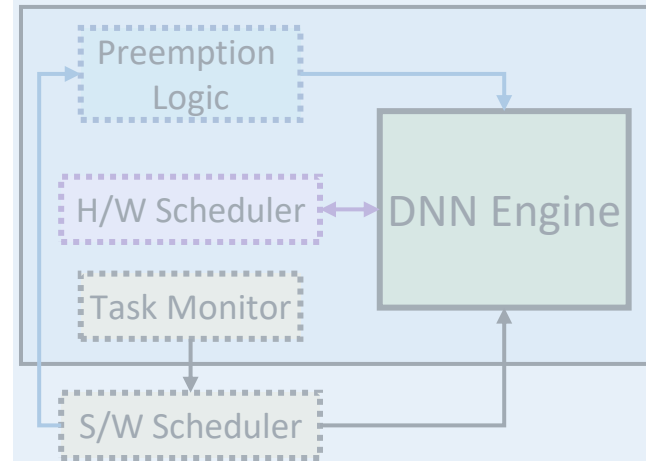
- Key design decisions

- Inter-DNN parallelisation strategy →
- DNN Engine Architecture →
- Scheduling →

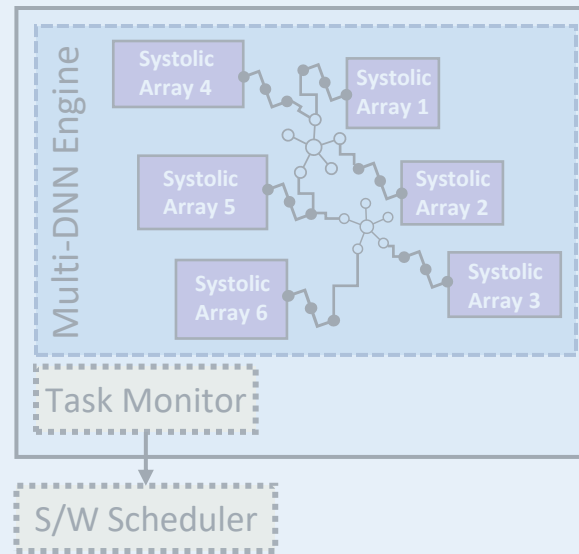
Approach 1	Approach 2
Time-mux	Spatial Co-location
Enhancing existing architectures	Custom Designs
Static	Dynamic

Landscape of Multi-DNN Accelerators

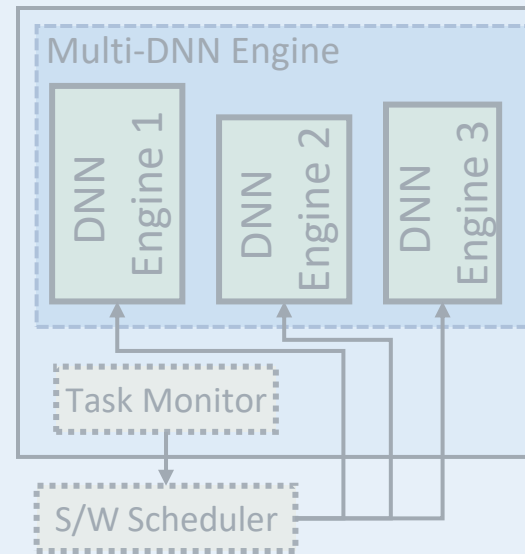
*(a) Single-DNN Engine
time-mux*



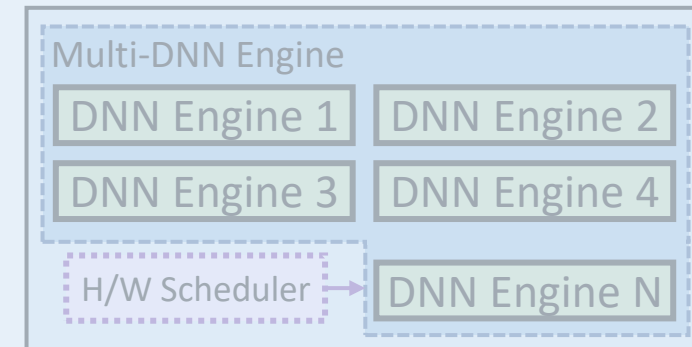
*(b) Composable Engines
time-mux &
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*(c) Heterogeneous Engines
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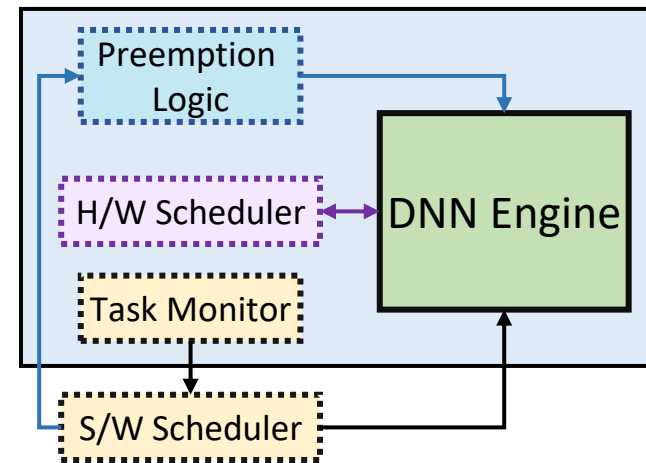


Programmability

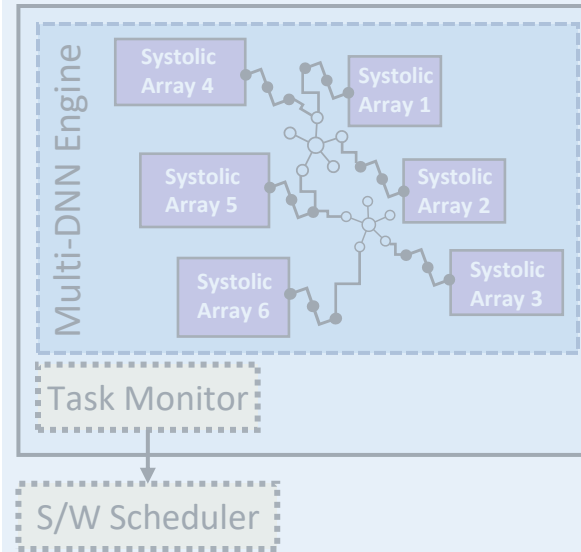
Customisation

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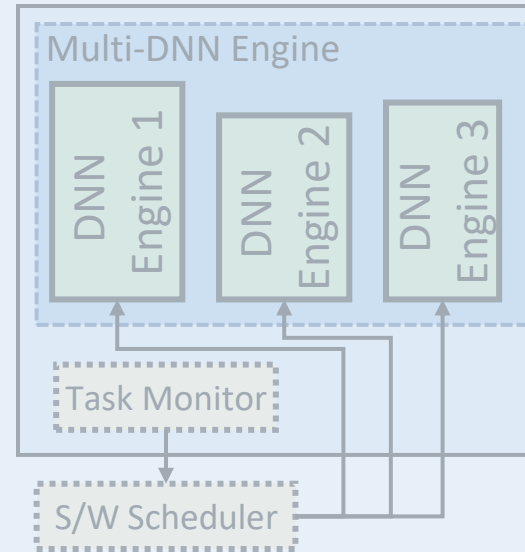
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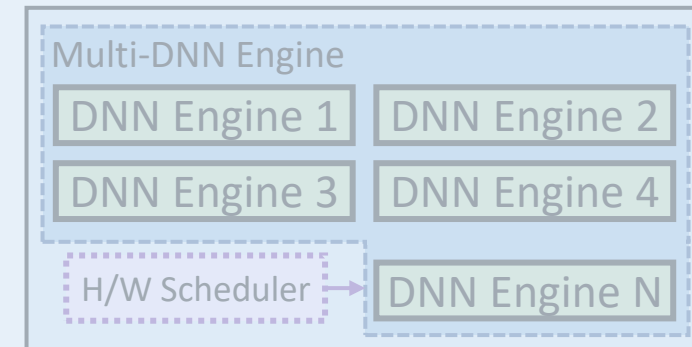
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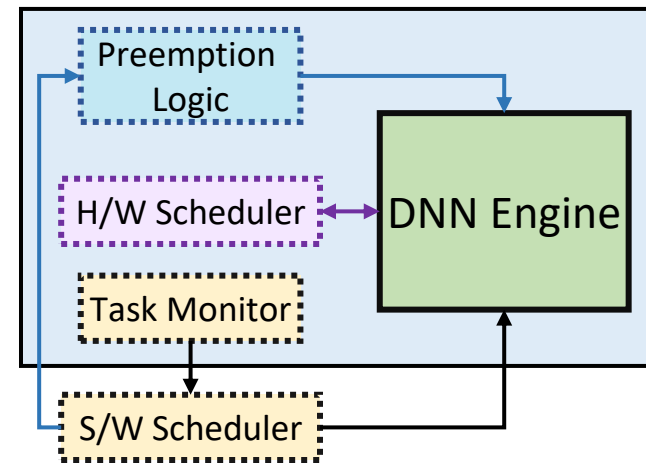


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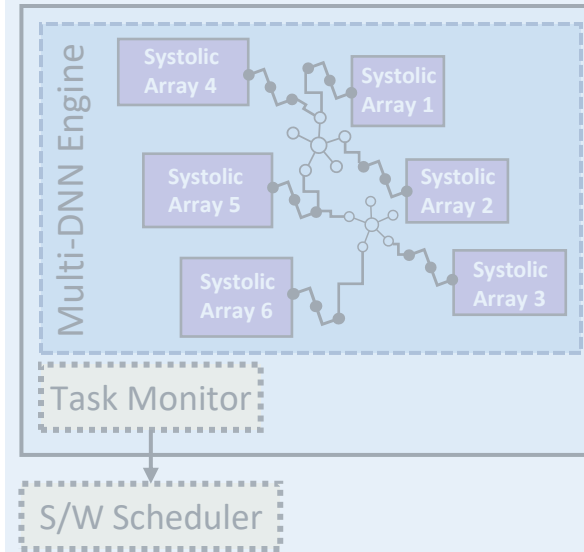
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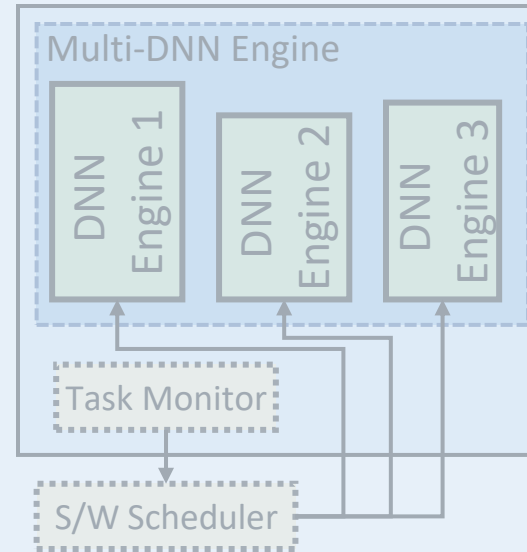
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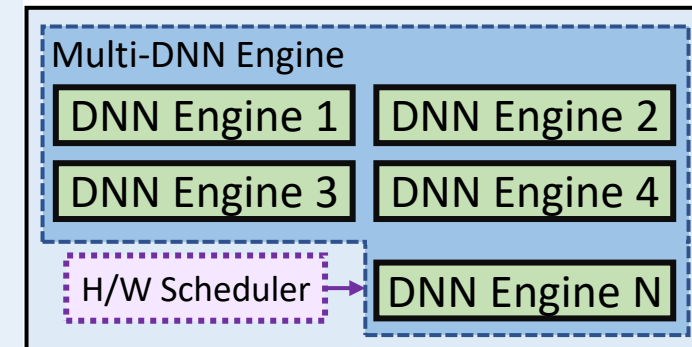
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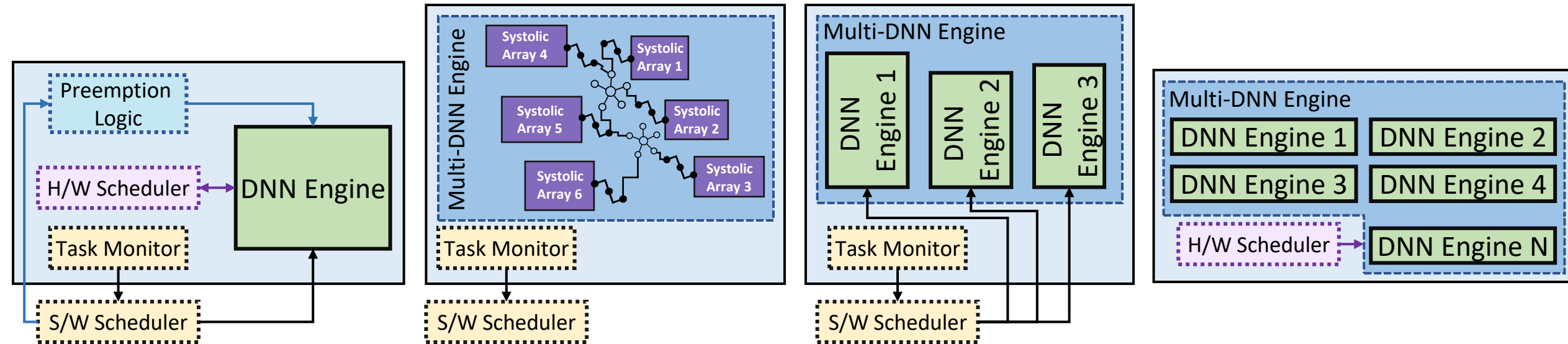


Programmability

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Landscape of Multi-DNN Accelerators

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time-mux
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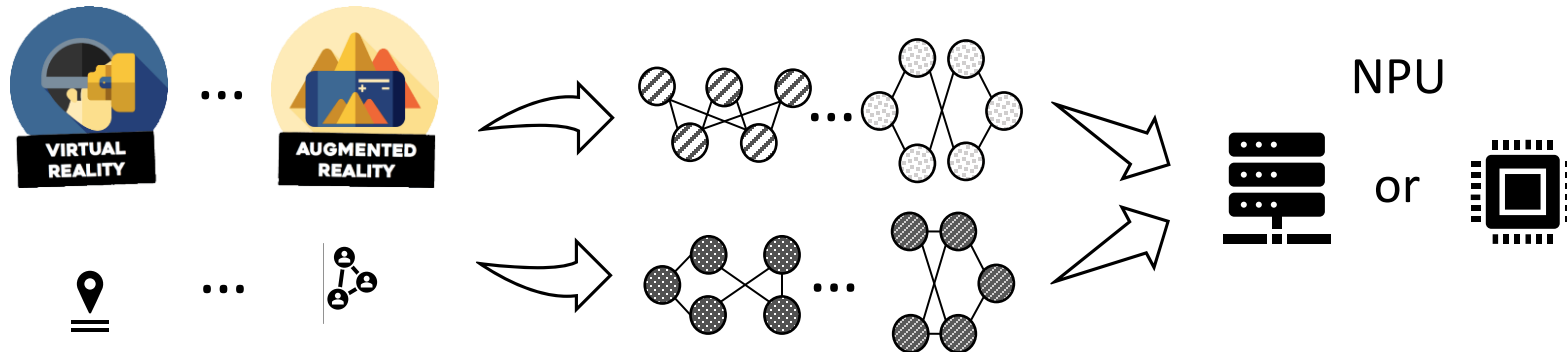
Programmability

Customisation

Case Study: Sparse Multi-DNN Workloads

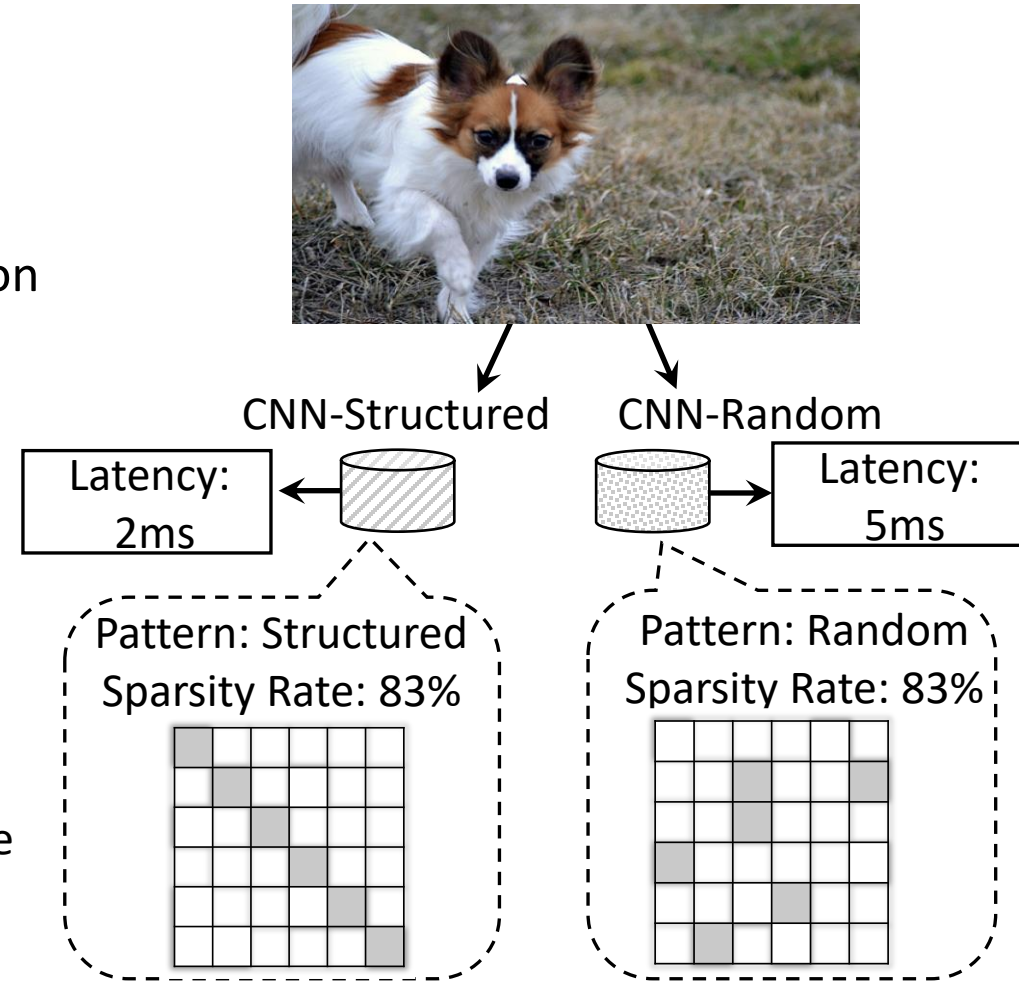
- Sparse multi-DNN workloads
 - Different sparsification methods, e.g. channel-wise, N:M block-wise, random
 - Diverse inference requests: <input, DNN, sparsification method, KPI>
- Key component: Scheduling
 - Determine the execution order of multi-DNNs
 - Focus on layer-wise execution on the NPU

Input user requests



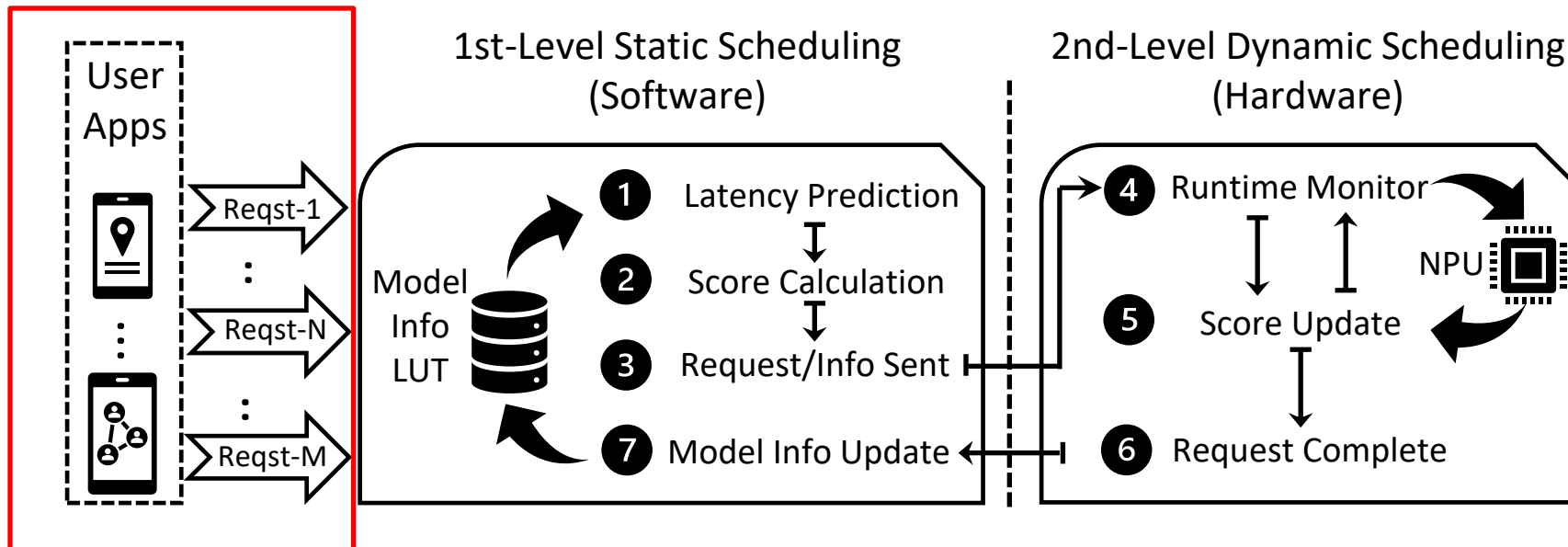
Case Study: Sparse Multi-DNN Workloads

- Current approaches
 - Lack of adequate sparsity support
 - Only consider average sparsity rate
- Untapped opportunity: Fine-grained sparsity information
 - Sparsity pattern
 - Sparsity dynamicity
- Sparsity pattern → hardware efficiency variability
 - NVIDIA Tensor Core: N:M block-wise sparsity
 - Samsung Exynos NPU: Random sparsity
- Sparsity dynamicity → Runtime variance
 - Varied latency performance can affect the best schedule



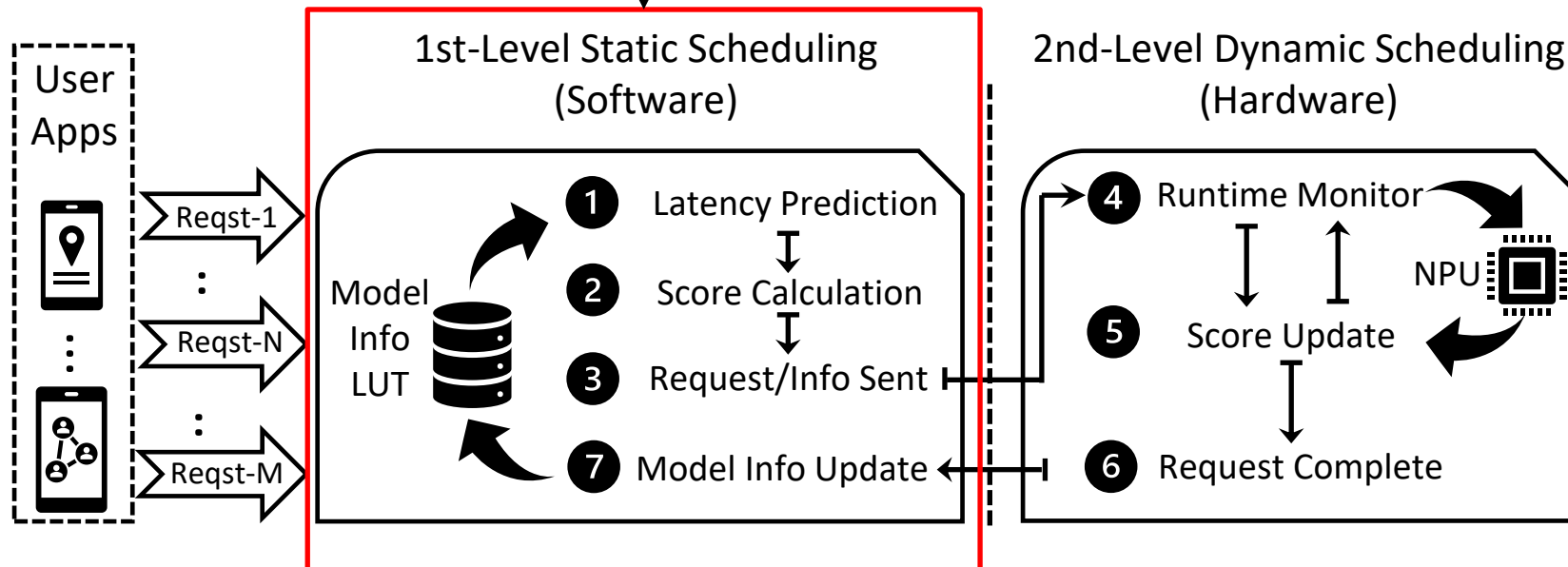
Case Study: Dysta

- **Problem:** Schedule variably sparse DNNs on zero-skipping NPUs, when each request has different <input, DNN, sparsity pattern, runtime sparsity level, KPI>
- **Approach:** Sparsity-aware bi-level scheduling
 - Capture both **sparsity pattern (static)** and **dynamic sparsity (run-time)** information
 - SW-based static scheduler: Initial schedule
 - HW-based dynamic scheduler: Run-time schedule refinement



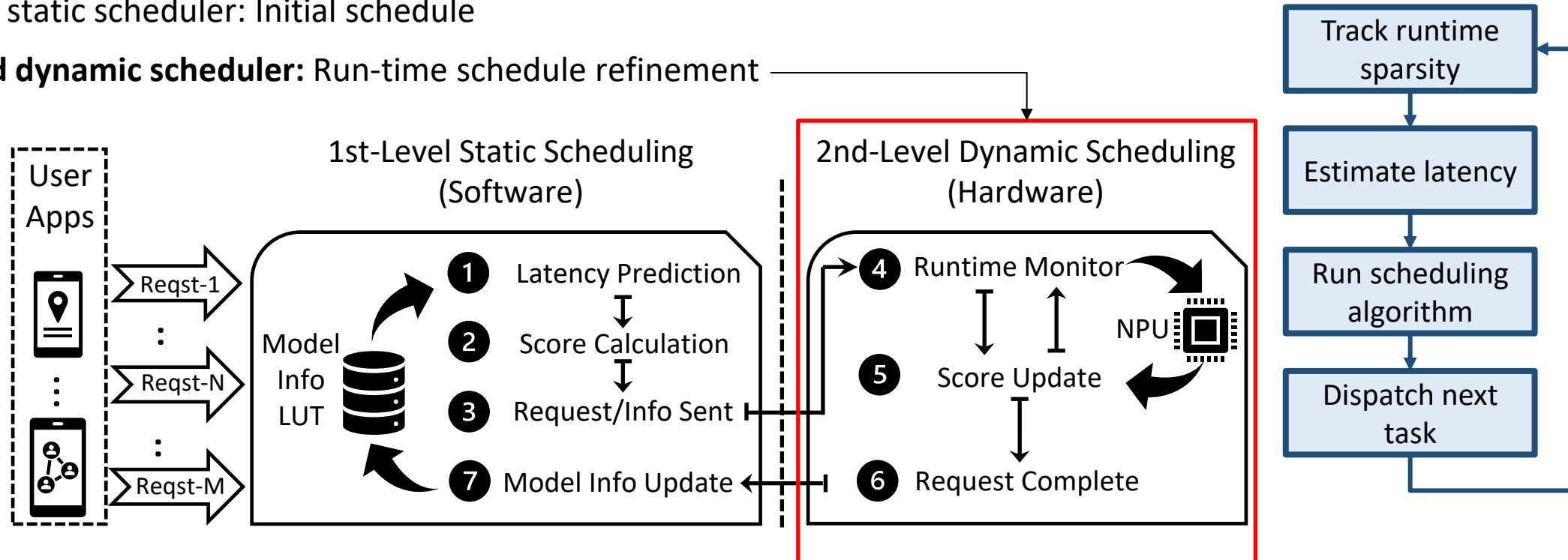
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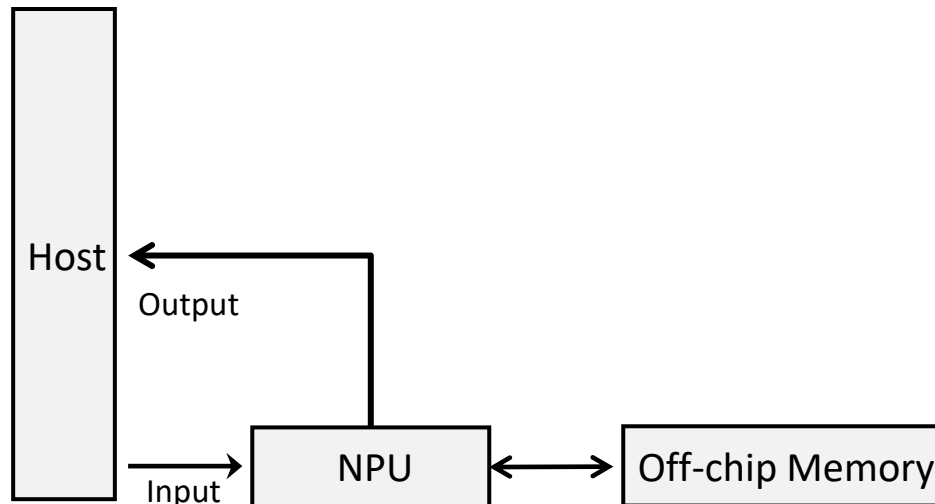
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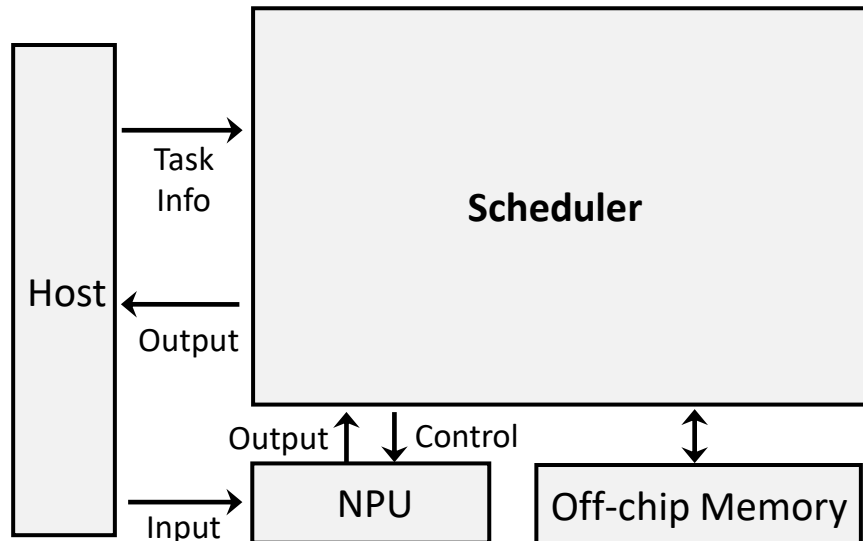
Case Study: Dysta – Enhancing existing NPUs

- Hardware scheduler
 - FIFOs: Track per-task information
 - Monitor: Track runtime sparsity
 - Compute unit: Estimate latency and update schedule
 - Reconfigurable design: Reuse resources for latency estimation and scheduling algorithm

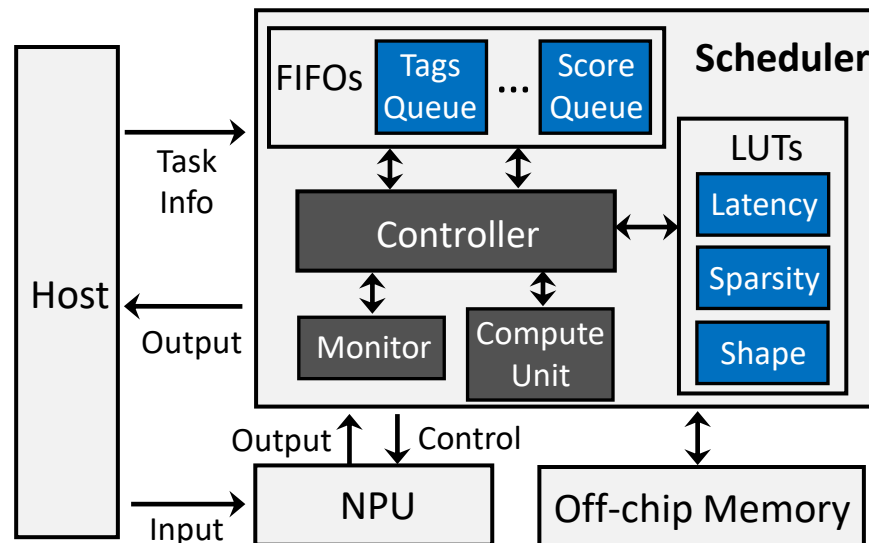


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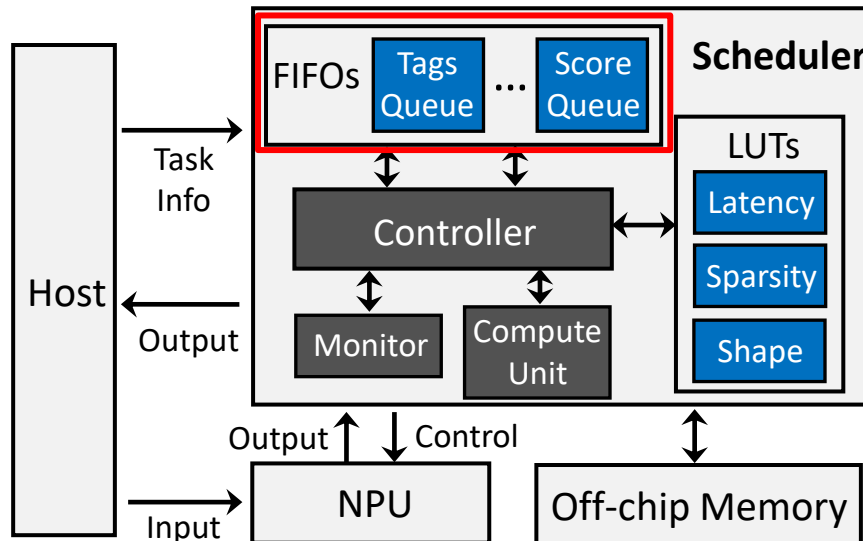


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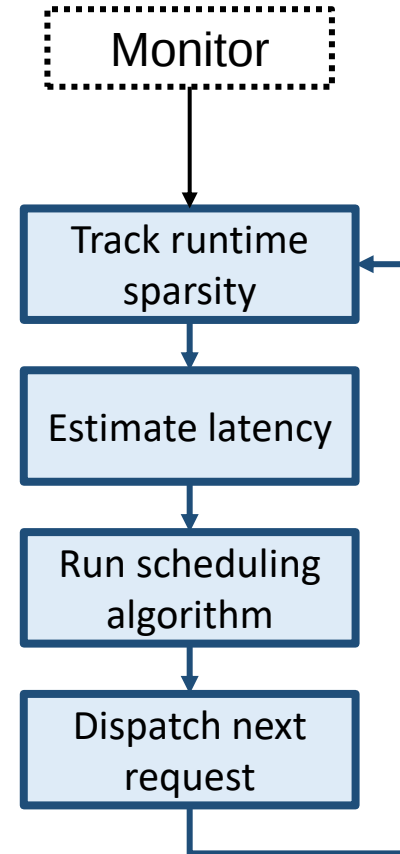
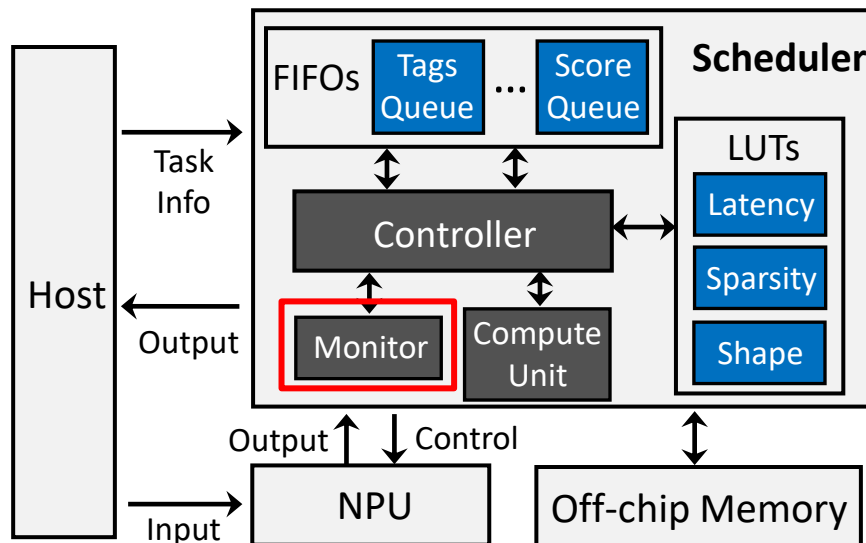
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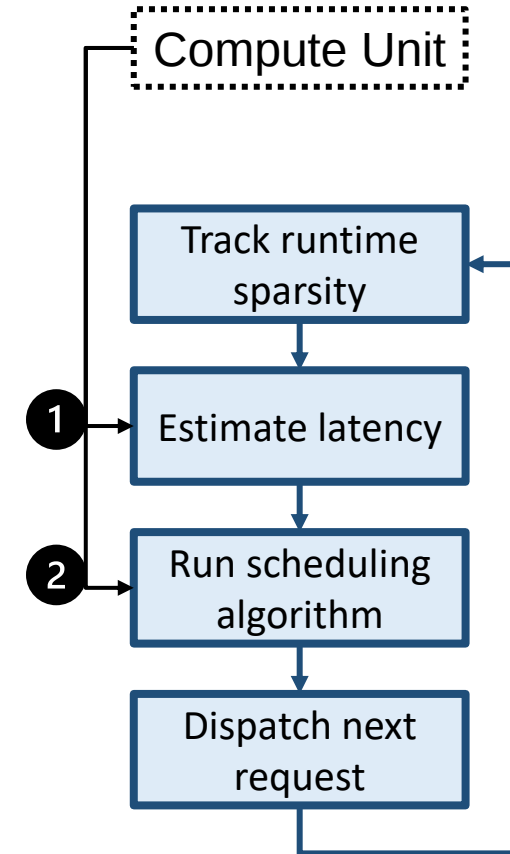
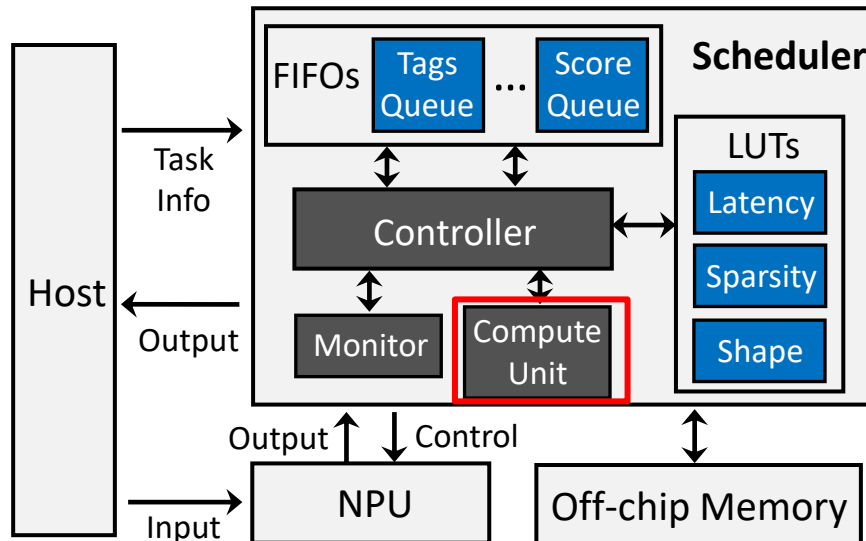
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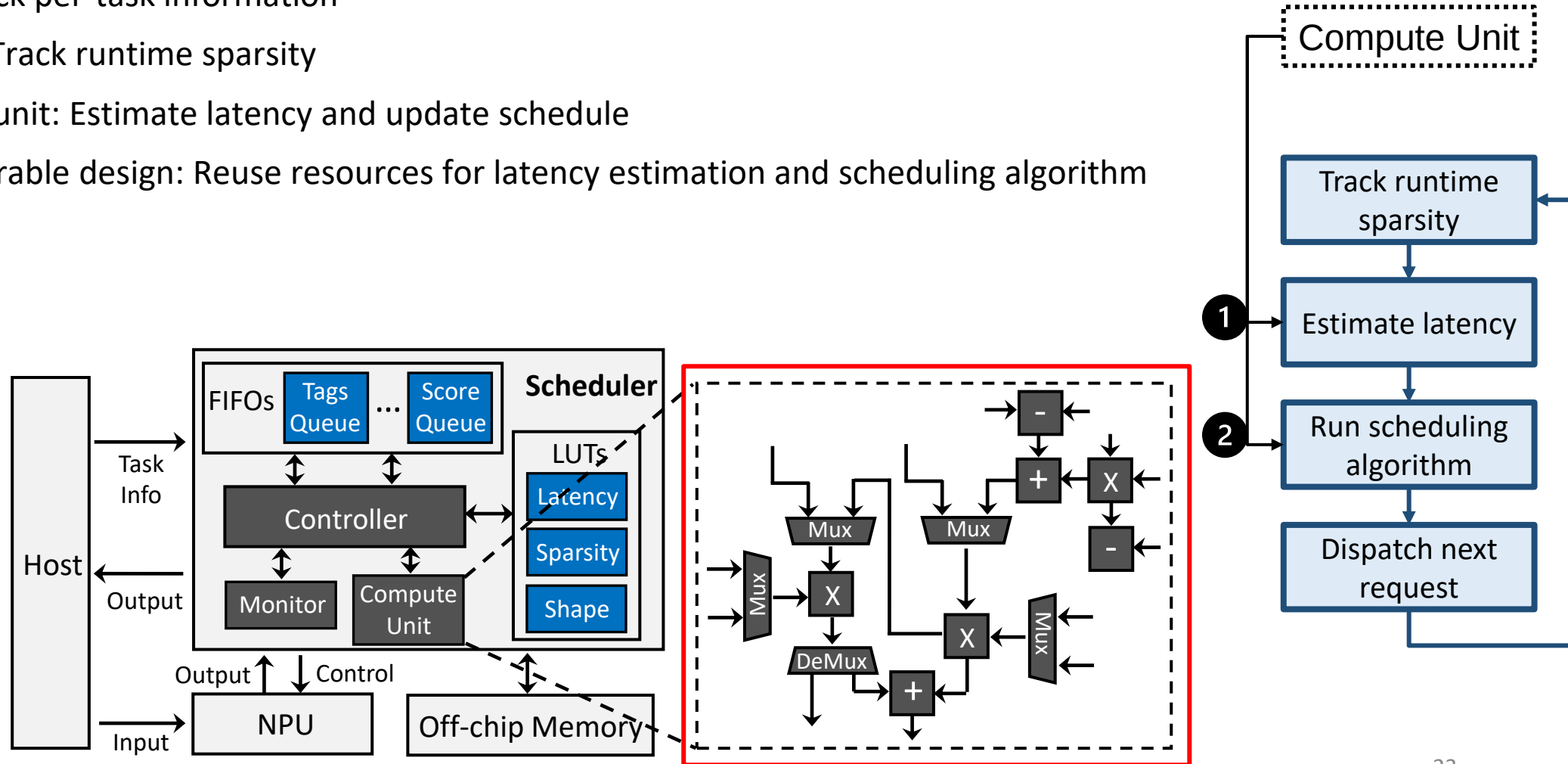
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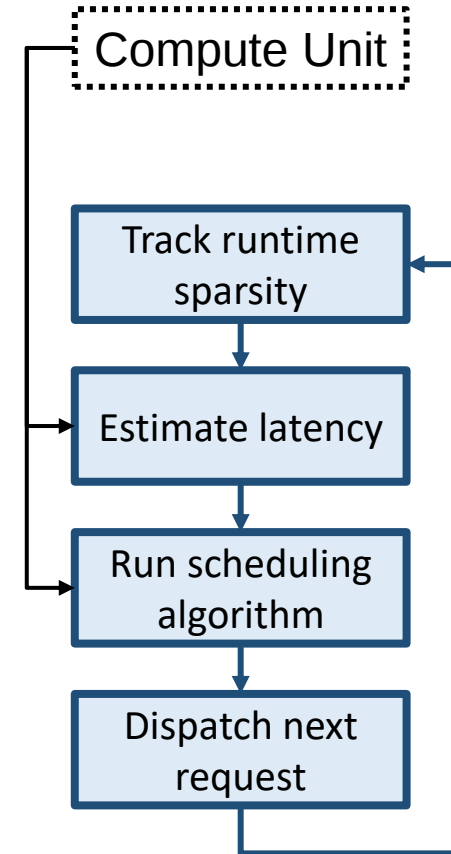
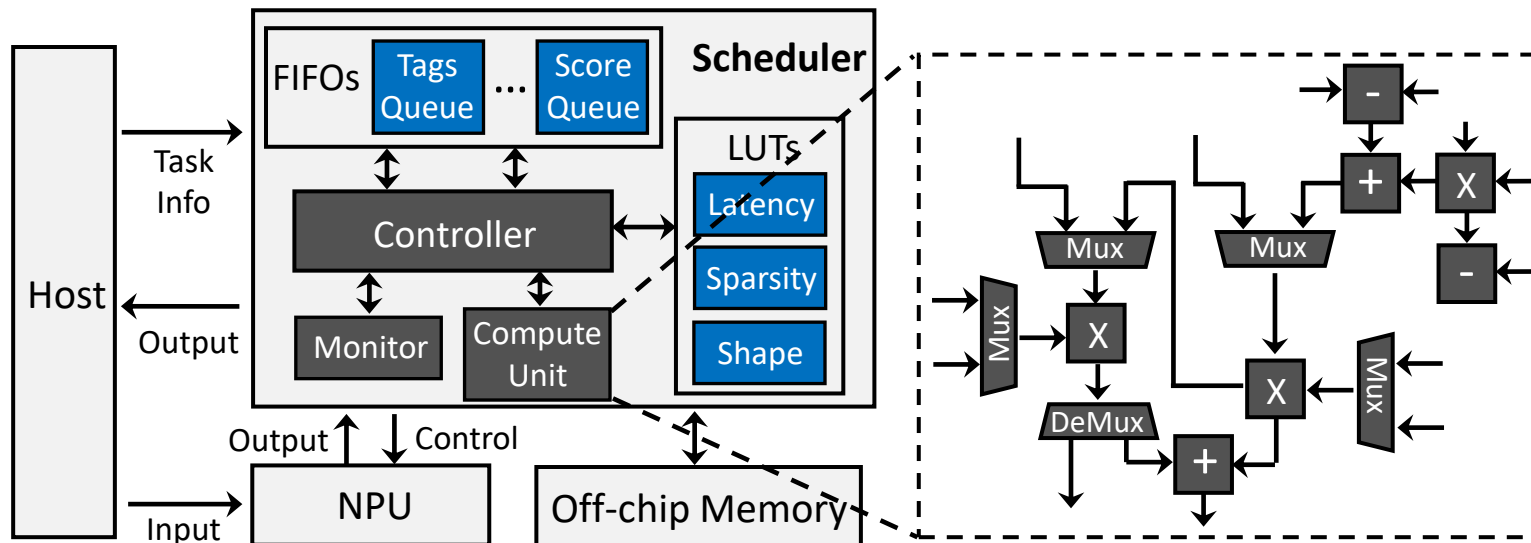
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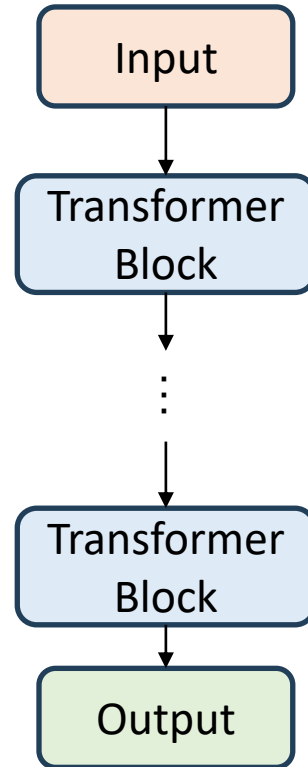
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- Hardware scheduler
 - FIFOs: Track per-task information
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 - Reconfigurable design: Reuse resources for latency estimation and scheduling algorithm
- Up to 10% lower latency constraint violation rate and nearly 4x lower average normalised turnaround time across request traffic levels over state-of-the-art methods



Future Trends & Open Questions

- Foundation models
 - Powerful pretrained models
 - Parameter-efficient Fine-tuning (PEFT) to downstream tasks
 - **Frozen shared part & task-specific adaptation part**

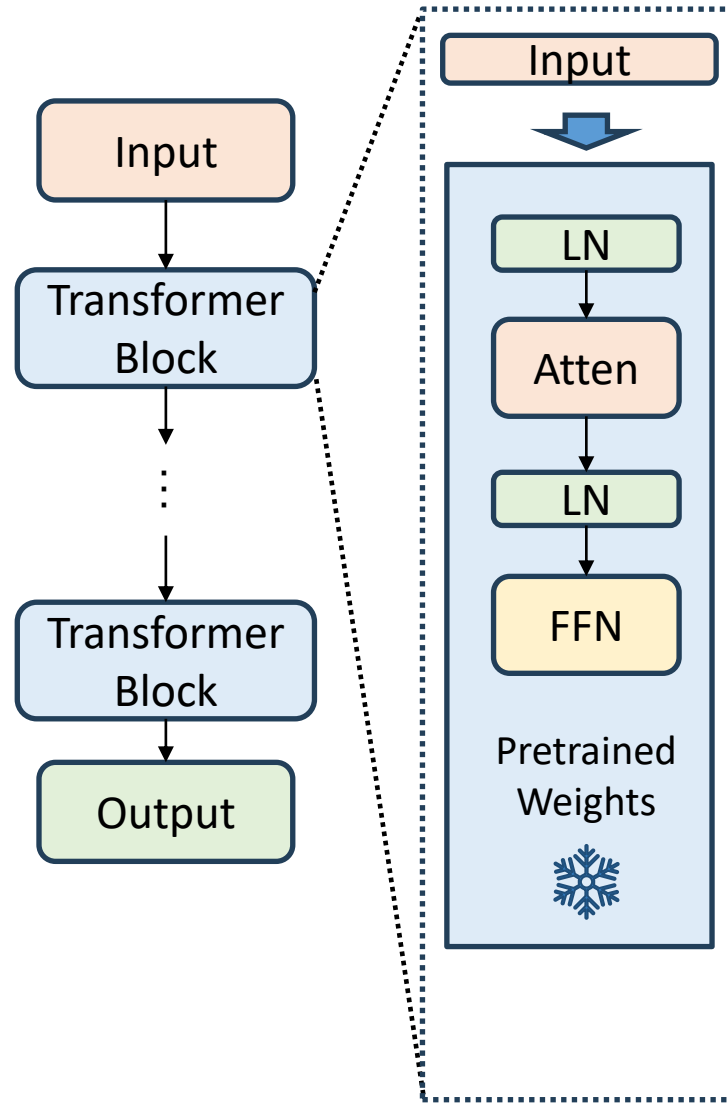


[2] L. Chen, et al. Punica: Multi-Tenant LoRA Serving. *MLSys*, 2024.

[3] Sheng, Ying, et al. S-LoRA: Serving Thousands of Concurrent LoRA Adapters. *MLSys*, 2024.

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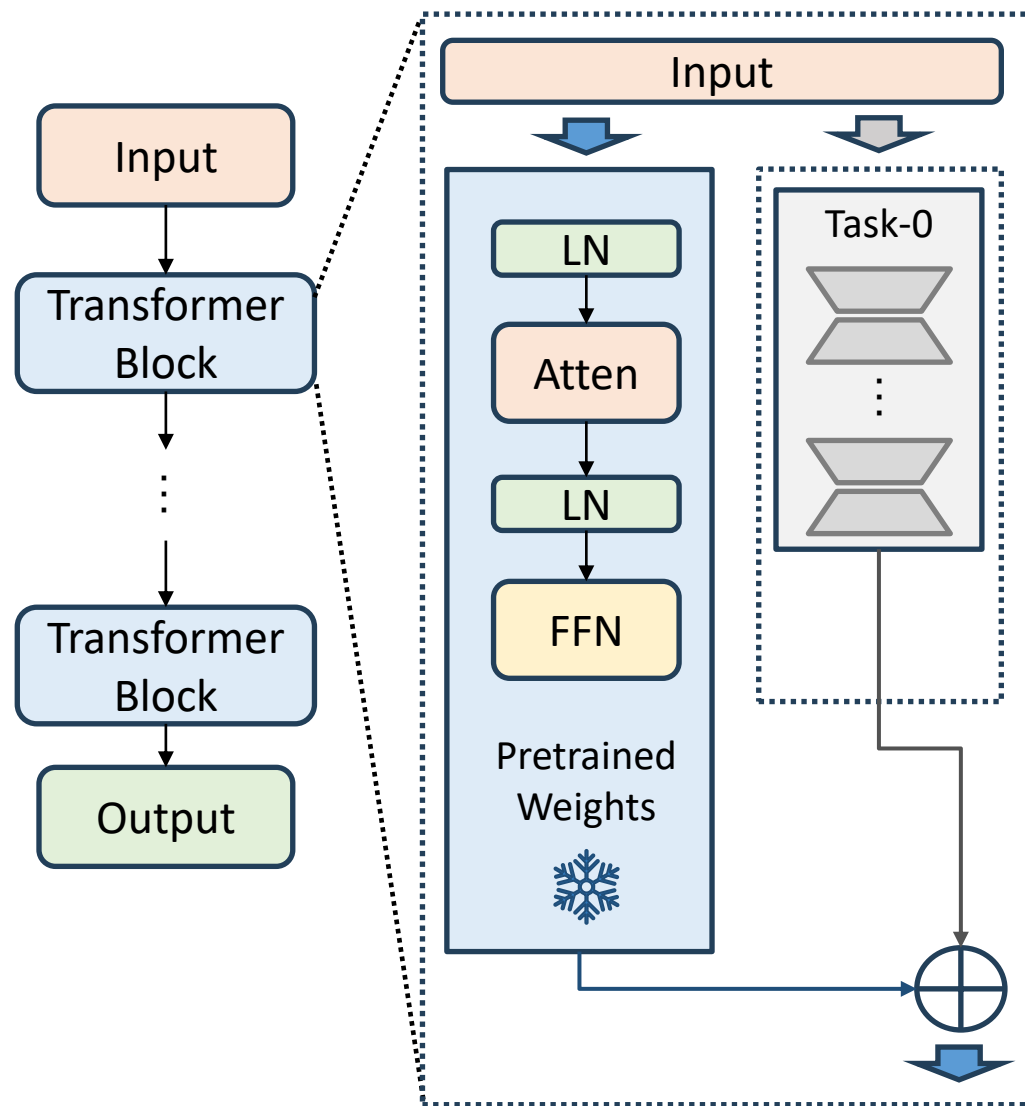


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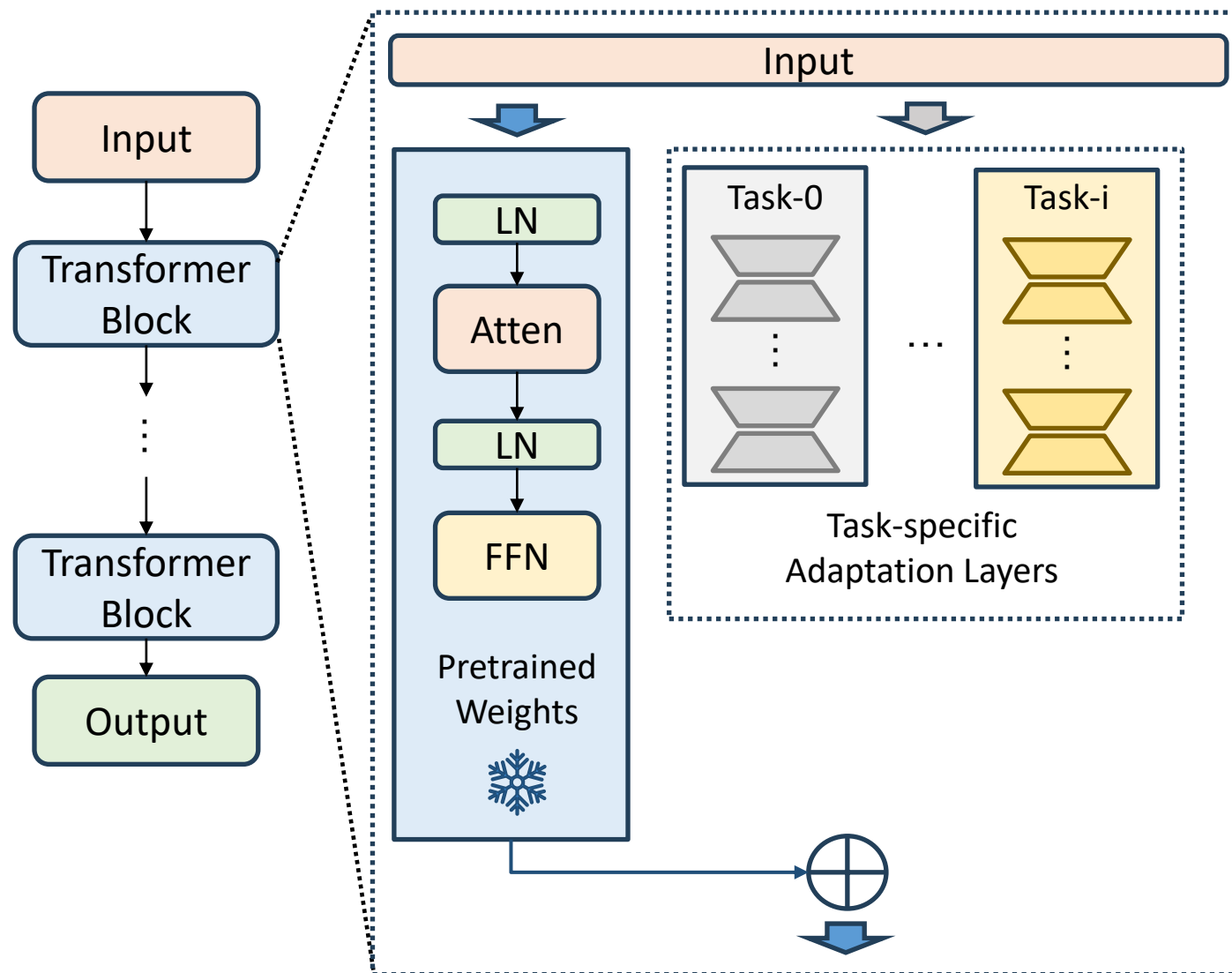


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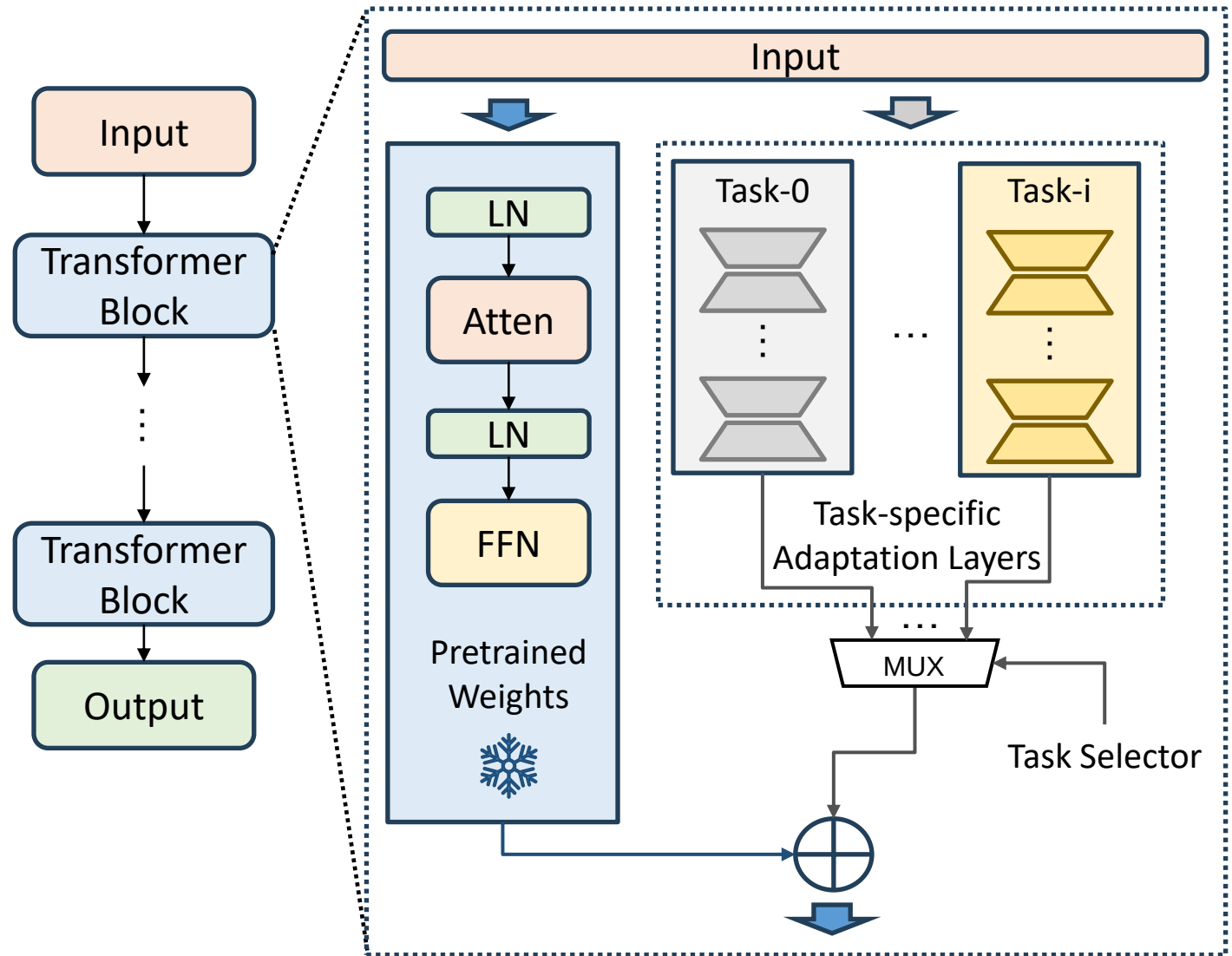


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 - **Frozen shared part & task-specific adaptation part**
- Research Questions
 - How to swap efficiently between Adaptation layers? Different memory management approach?
 - How to design the underlying hardware? Specialised units or unified for Shared and Adaptation parts?
 - Model-Hardware Co-Design for the next milestone



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Thank you

Multi-DNN Accelerators for Next-Generation AI Systems

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Nicholas D. Lane
University of Cambridge
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Sparse-DySta: Sparsity-Aware Dynamic and Static Scheduling for Sparse Multi-DNN Workloads

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