Survey of Nanoscale Digital System Technology

FCCM Evening Workshop

April 23, 2002

<u>Moderator</u>

Mike Butts - Cadence

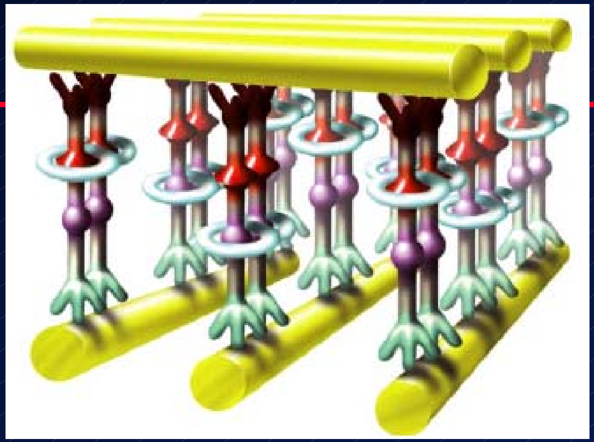
<u>Panelists</u>

Andre DeHon - Caltech

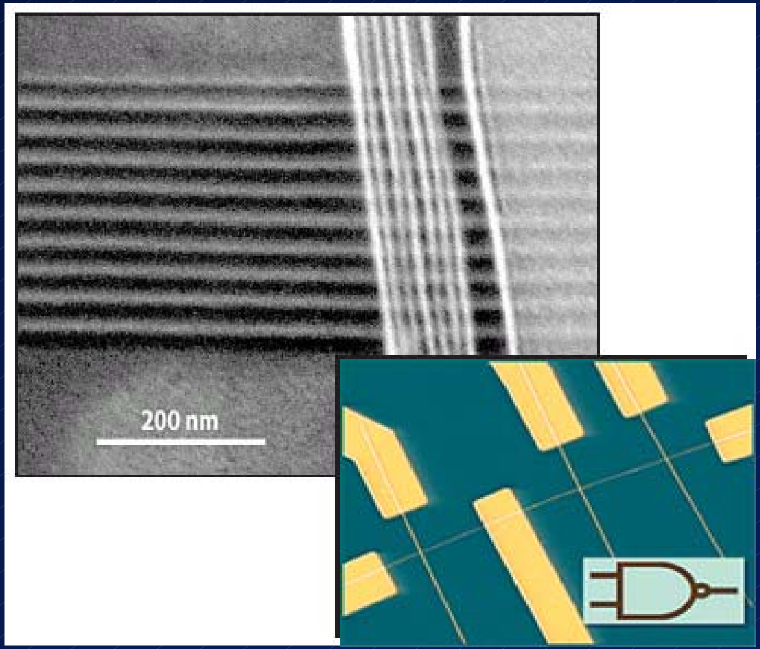
Phil Kuekes - HP Labs

cadence

Nanoelectronics is Coming



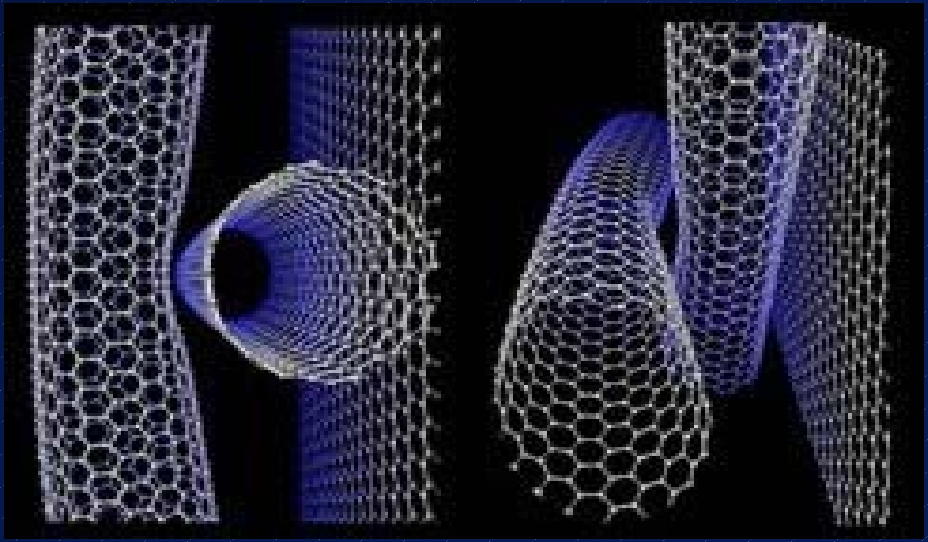
- Molecular-scale devices
  - programmable *only*
  - FPGA, NVRAM
  - up to 1 trillion devices / cm^2
- Mass-fabricated cheaply
- Solid lab results today
- Timeline?
  - 16 Kbit RAM: 2005
  - Niche products: 2008
  - = CMOS density: 2011



Carbon Nanotubes (NTs)

- Carbon sheet one atom thick, wrapped in a tube
- 1-5 nm wide, up to > 1 mm long
- NT is one molecule: extremely strong, flexible
- NTs are metals or semiconductors
  - Depending on their lattice geometry
  - No way to synthesize a pure batch so far
- NTs are very new (‘91), technology may improve

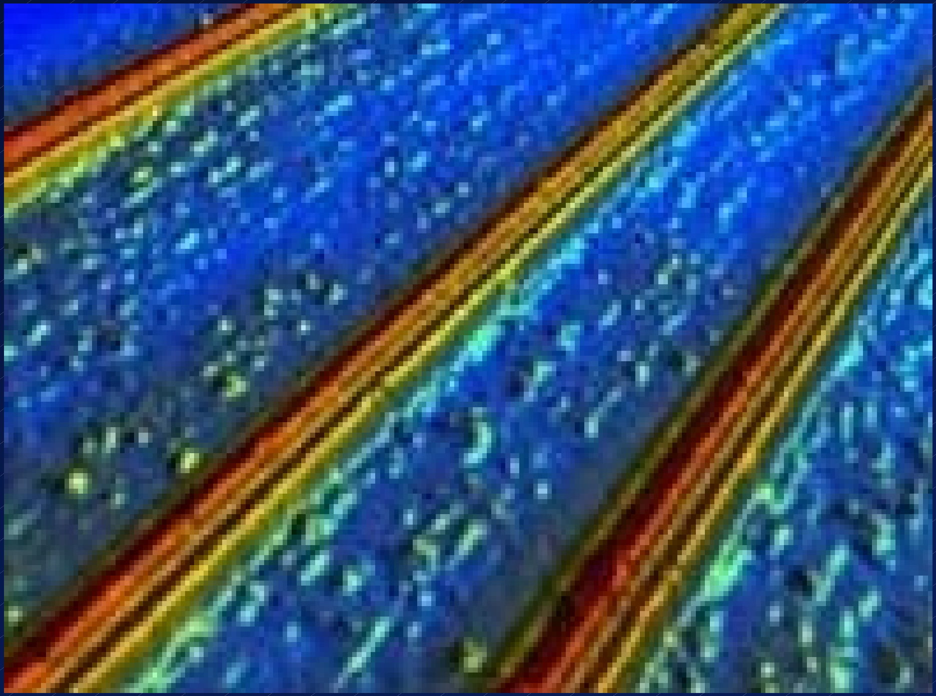
IBM



Silicon Nanowires (NWs)

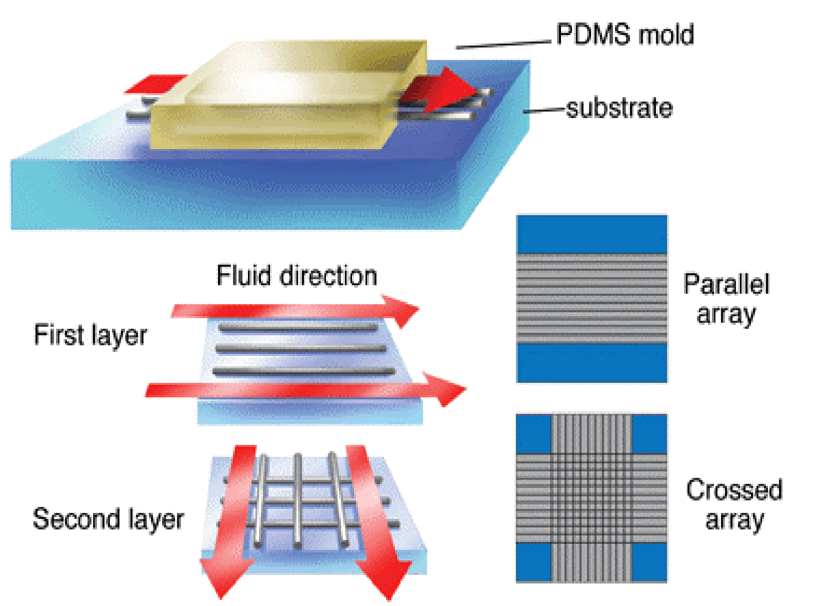
- Single-crystal silicon, 6-20 nm diameter, 1-30 μm long
- Fabricated in bulk by laser-assisted catalytic growth
- Ge, Au, GaP, GaN, InP NWs have also been made
- p-type and n-type NWs
  - Controlled doping with phosphorous and boron has been successful

HP



Fabrication: Bottom-Up Self-Assembly

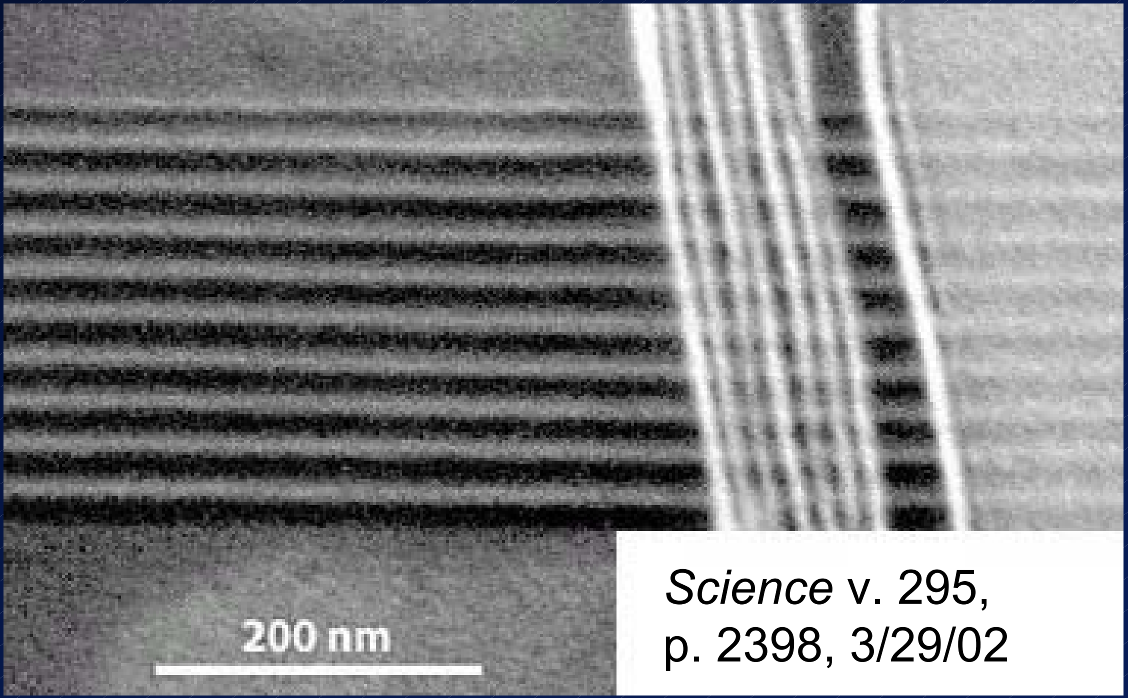
- We can't make nanocircuits *top-down*
  - Lithography can't go down to single molecules.
- So make them *bottom-up*, with chemical self-assembly
  - Their own physical properties keep them in regular order, like crystals do when they grow.
  - Tease nature into forming crossbars that we can program.
- Fluid flow self-assembly
  - Flow rate and duration controls wire separation
  - Crossbar in two passes



Science

Fabrication: Bottom-Up Self-Assembly

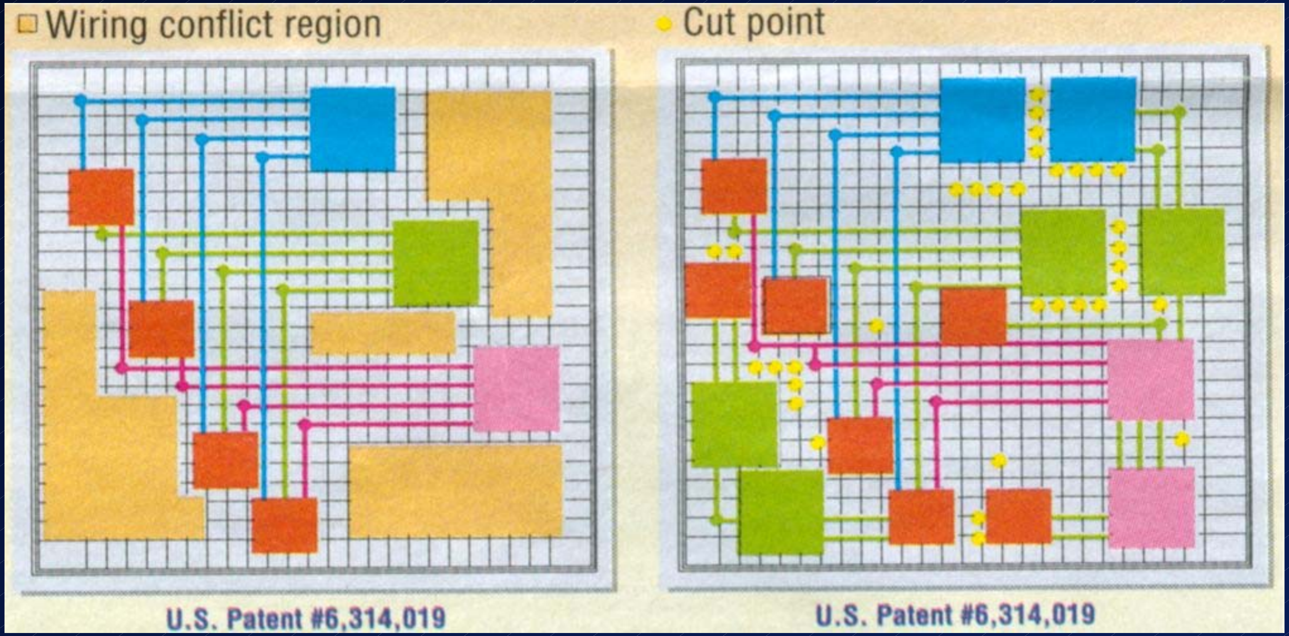
- Atomic superlattice used as a template for growing NWs by molecular beam epitaxy
- NWs transferred to substrate, repeated to make crossbar
  - Translates atomic control of film thickness into atomic control of NW diameter and spacing
  - Heath, Melosh group at UCLA



Science v. 295, p. 2398, 3/29/02

Post-Fabrication: Programmable Wire Cuts

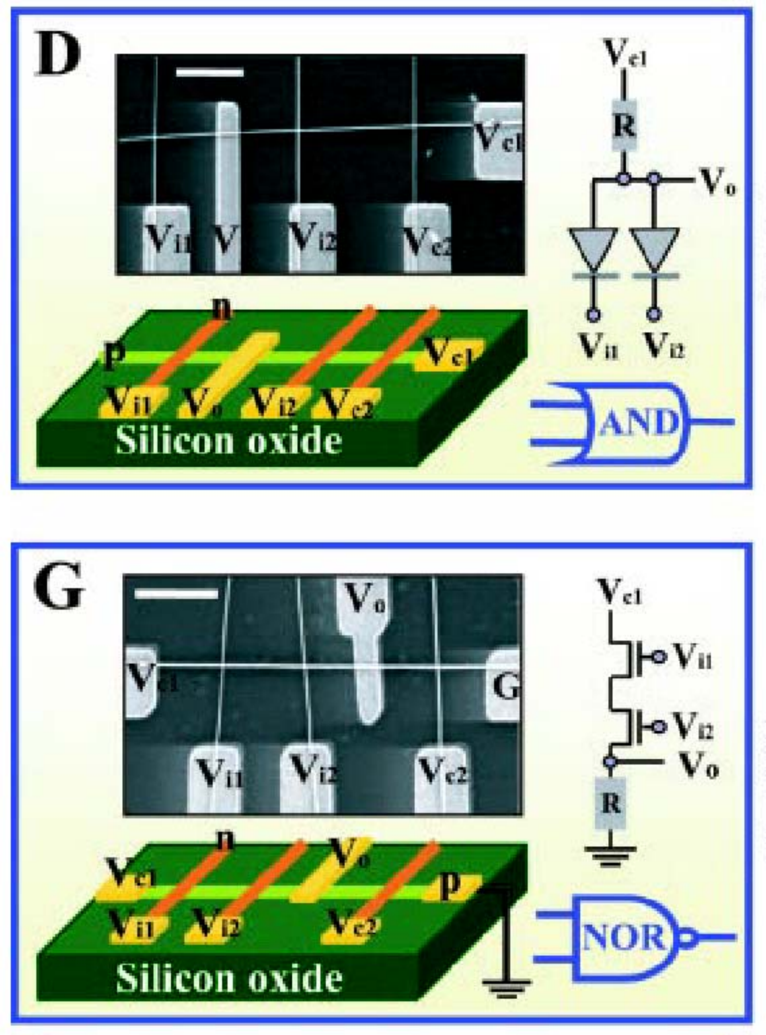
- Crossbar wires can be cut with programming voltage when molecular switches are used at the crosspoints.
- Voltage over-oxidizes the switch, breaks the nanowire
  - NW is small enough to be consumed by the chemical reaction.



EE Times

Devices: Transistors and Diodes

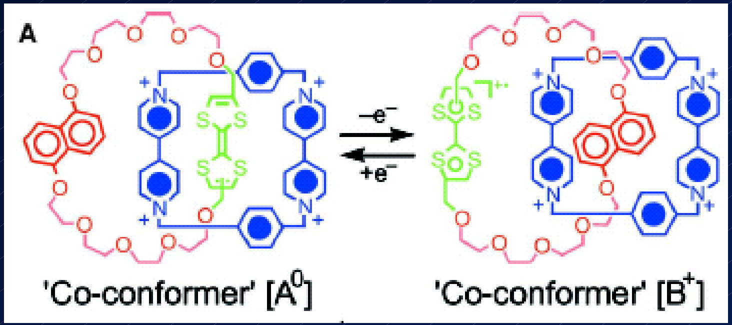
- Cross two doped NWs: diode
  - 90% yield, 1V turn-on, AND gate:
  - addressable crossbar diode array
  - high V makes it high turn-on (open)
- Oxide between NWs: FET
  - p-Si NW channel, n-GaN NW gate
  - voltage gain = 5, NOR gate:
  - also programs open with high V
- Single-molecule FET channel
  - reported by Bell Labs (!?)



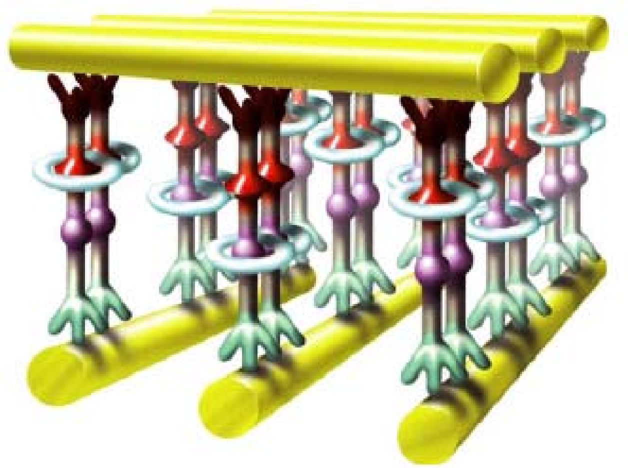
Huang, et al

Devices: Molecular Switches

- Organic molecules with two parts
  - ring and rod, interlocking rings
- Programming voltage shifts it
  - changes its conductivity
- Non-volatile programmable switch
- [2]Catenane
  - 2V: opens it, -2V: closes it, many cycles
  - 4X difference, OK for memory
  - p-NW/NT array: programmable diodes
- Better molecules coming

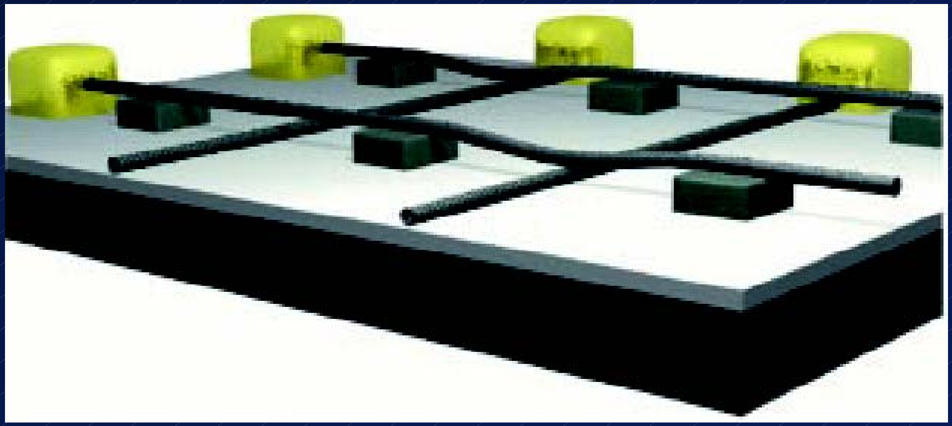


Science



Devices: Mechanical Switches

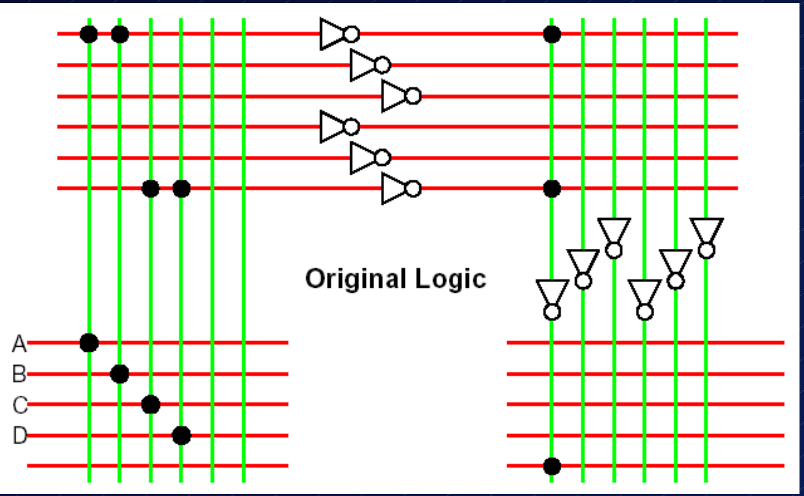
- NW/NT crossbar, upper half suspended over lower half
- Programmable array of non-volatile bistable switches
  - Charge attracts wires to touch, van der Waals force sticks them
  - Opposite charge opens them back up
  - Has been simulated, one switch works in the lab
- Diode array is a RAM
  - lower half semiconducting NWs or NTs should make diodes at contact points
- Programmable FETs?
  - upper NT is gate or open

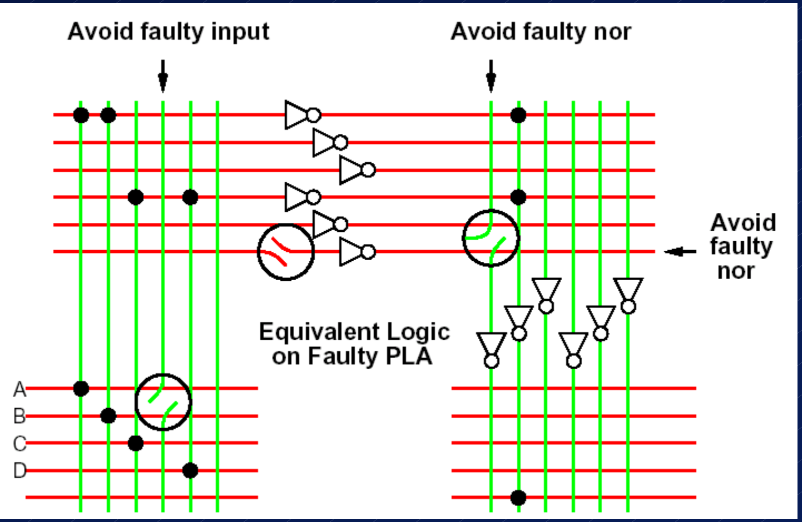


Rueckes, et al

Implications of Bottom-Up Fabrication

- Defect-tolerance is Required
  - Nature of chemical processes
  - Alignment at single molecules
- Design by Programming
  - FPGA with lots of spares
  - Tested and programmed to avoid defects
- Cheap fab, Cheap gates
  - Batch chemical processes make regular materials
  - Fabrication cost per device practically zero





DeHon

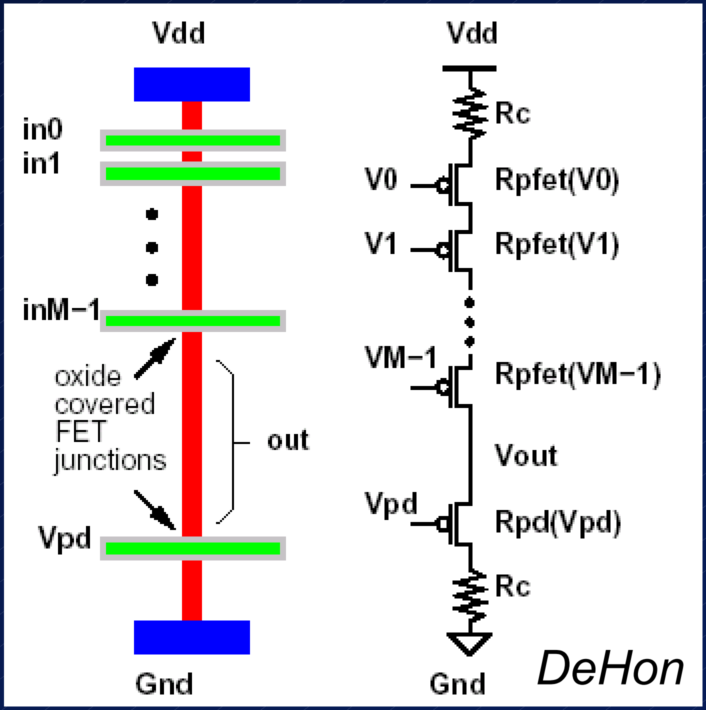
Large Defect-Tolerant Systems

- Teramac: reconfigurable computing system built by HP Labs, mid '90s
- 8 boards, 32 MCMs, 864 FPGAs.
- 75% of the FPGA dice, 50% of the MCMs, and 10% of the inter-chip signals were defective
- Developed methods for
  - Detecting defects in programmable HW
  - Using FPGA programming to compile around the defects
- Years of reliable operation

Logic and RAM Candidates

- Two-terminal devices: self-assembled crossbars
  - Molecular switch with diode: read/write, too much leakage?
  - NW-diode: one-time-programmable (OTP), less leakage
  - Mechanical switch with diode:

    zero leakage, read/write, fab?
  - Restoring NW-FET buffers required
- NW-FET NOR crossbar arrays:
  - Self-restoring, OTP, static power
- Non-volatile RAM
  - R/W molecular or mechanical switch crossbar arrays are ideal



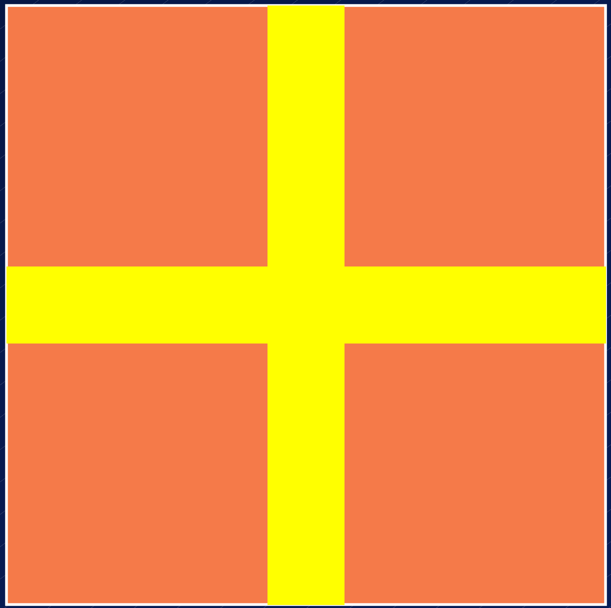
Vastly superior crosspoint density

- CMOS crosspoint costs about 8 transistors area
  - SRAM cell, big n-channel pass transistor
  - Far larger than minimum feature pitch
- NW or NT crosspoint fits inside the wire crossover
- Area for one crosspoint switch: 625X

25nm nanowire pitch
$(25nm)^2$

100nm

25nm CMOS process
$(625nm)^2$

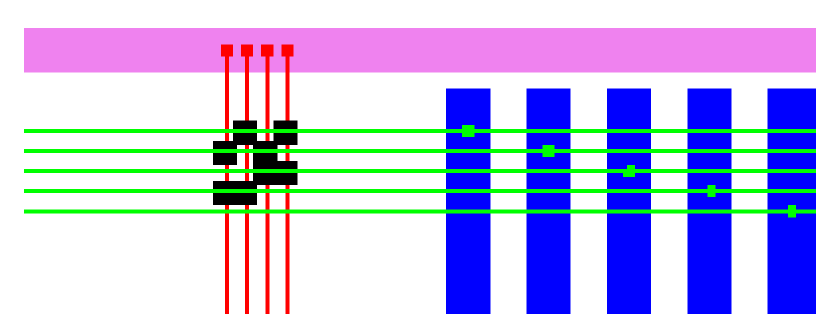


- NanoFPGAs are very attractive
  - Fully populate crossbars: rich routing

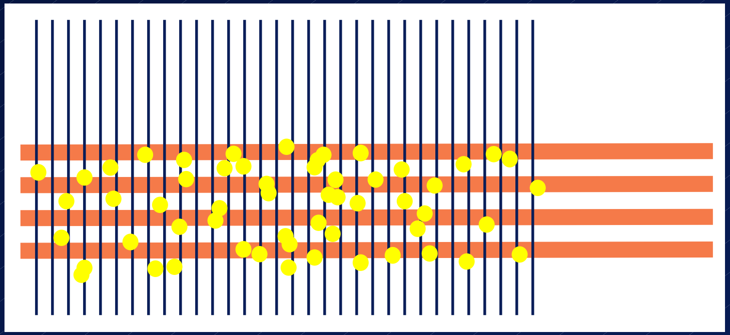
ref: DeHon 2002

Interface to Microelectronics

- Nanoelectronics must interface to microelectronics.
  - Can't position individual features at nanometer scale.
- Connect log(N) microwires to an orthogonal set of N nanowires (i.e. log(N) = 10, N = *1000)*



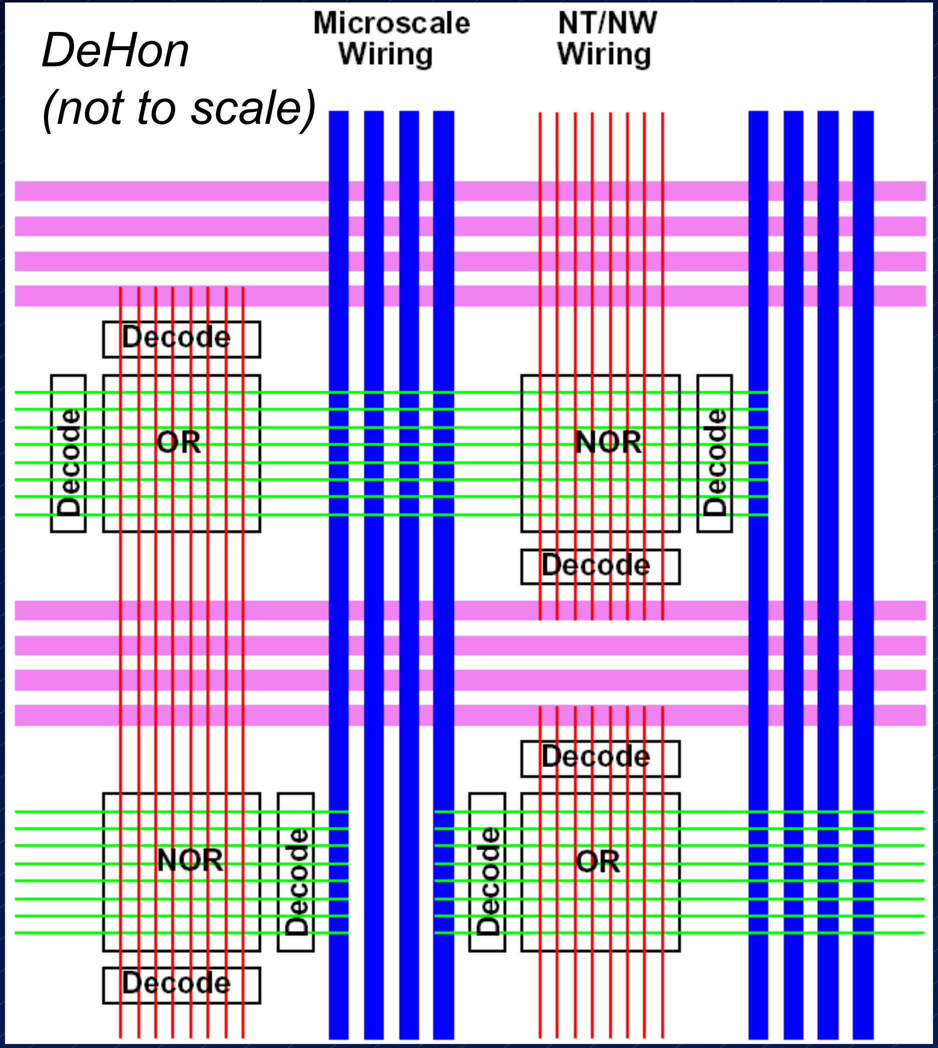
DeHon: Patterned stamped mask



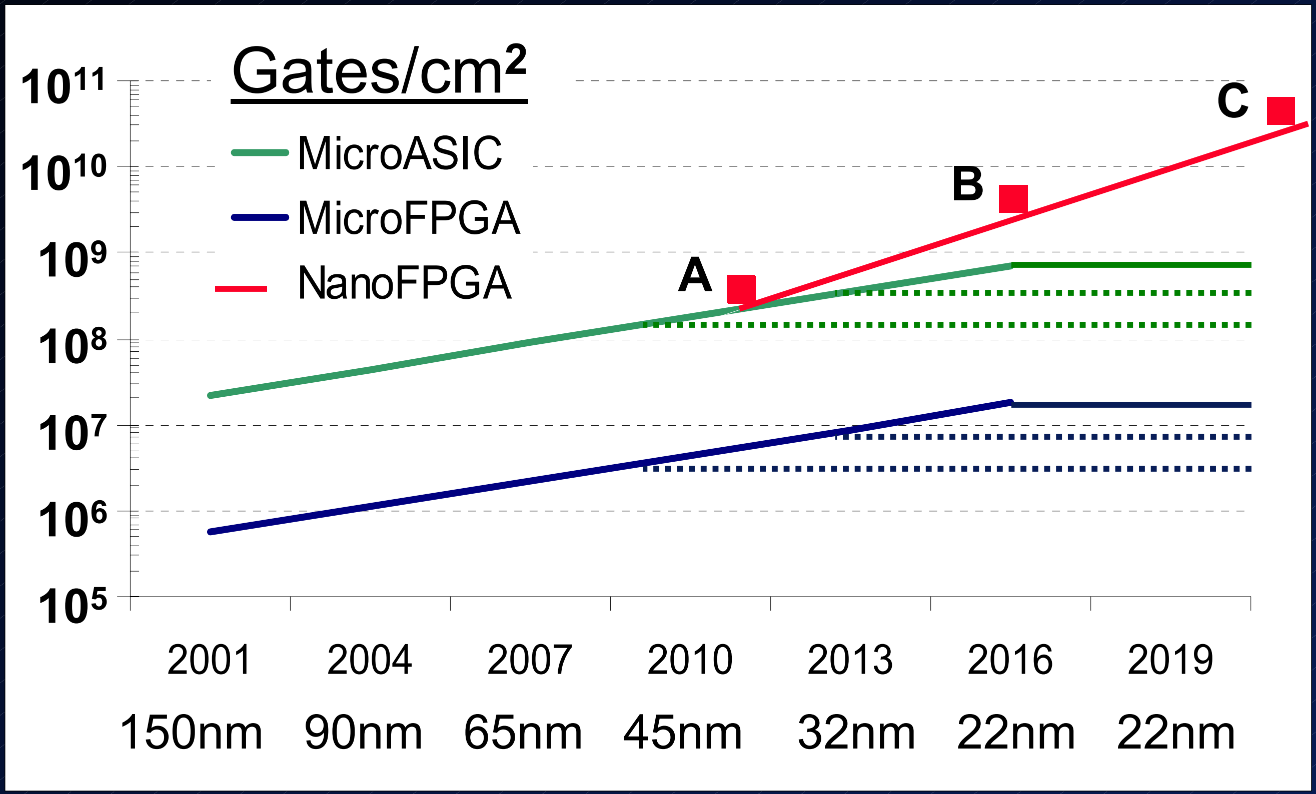
HP Labs: Random gold dots

System-Level Interconnect

- Programmable OR/NOR, NVRAM nanoarrays
- Interconnect arrays by
  - Extending NWs across multiple arrays, or
  - Through fully populated interconnect crossbars
  - NW-FET buffer/registers in-between when needed
- Interface to microwires with *N*-log(*N*) decoders



Logic Density Projections



NanoFPGA

- **A**: 50nm pitch, 20% utilization: 400 million G/cm^2
- **B**: 25nm pitch, 50% utilization: 4 billion G/cm^2
- **C**: 10nm pitch, 80% utilization: 40 billion G/cm^2

- MicroASIC = ITRS 2001 roadmap
- MicroFPGA = 8 transistor-area/crosspoint, 20 crosspoints/gate
- NanoFPGA = 20 crosspoints/gate, assuming = ASIC in 2011, Moore's Law

Potential Roadblocks

- Power: 10^{11} devices/cm^2 * 1 nanowatt/device = 100 watts/cm^2
  - Static: almost any leakage is too much, Dynamic: $10^{11} * CV^2f$?
- Signal integrity: Crosstalk?
- Quantum effects? Electrons can act like waves too.....
- Reliability
  - Creeping defects after fab? Cosmic ray damage?
- Programming effort
  - Work around defects to get a defect-free generic array
  - Else, place & route a billion gates for each chip you make!

Workshop Topics

- What will these programmable gigagate nanoscale FCCMs look like? How likely is all this? When?
- What algorithms and software tools will we need to produce and use them?
- What topics should FCCM systems research (outside the chem labs) work on to help this all along?

Workshop Conclusions...............

FCCM: Faulty Chemical Custom Machines

- Testing in-place
  - Processors in the substrate, migrate into the array
- Defect tolerance model: DRAM? Disk?
- Fix defective real array into a generic good array?
- Incremental / in-place place&route
- Clocking and its implications
  - Asynchronous
  - QM: quantum resistance: maybe linear RC delay, not quadratic?
  - Micron-size clock domains
  - Clocked signal restoration / clock == power?

How to design a billion gates?

- Learn how to use large scale spatial processing
- Models of computation: abstracting up
  - Above Verilog/VHDL for heavens’ sake
- Alternate design forms? Bottom-up design
  - Neural, genetic, associative
  - The inverted V: HW – system SW – application SW

Does Cheap Gigagates make any fundamentally new problems solvable?

- Macro-scale massive computing
  - Holodeck-scale simulation,
  - safety, protection
  - ambient intelligence
- Micro-scale processors (100 MIPS in $(10\ \mu m)^{2)}$
  - power on ambient light
  - Biosensors, ‘fantastic voyage’ microsurgery
  - entertainment, weapons?