Survey of Nanoscale Digital System Technology

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ABSTRACT

The AAAS journal *Science* chose Nanocircuits as its Breakthrough of the Year for 2001 [27]. Last year's ICCAD keynote speech and evening panel were on Nanotechnology and Information [16]. Exciting results in basic research on molecular-scale electronic devices and interconnects are being reported with ever-greater frequency. Self-assembling digital systems with billions of components may be an engineering possibility in this decade. That would be just in time, as silicon photolithography sooner or later will reach physical and financial limits. Such a shift in electronic technology would be at least as profound as the shift from vacuum tubes to integrated circuits. This paper presents a survey of current research on molecular-scale electronic devices and interconnects, and on early explorations into molecular-scale digital systems.

1 INTRODUCTION

A nanometer (1/1000 of a micron) is about ten carbon atoms long. A new technology for digital electronics is emerging, with features in the 1 to 50 nanometer range, called nanoelectronics. Its molecular-scale devices and interconnects are made with carbon nanotubes, single-crystal semiconductor nanowires, and bistable organic molecules, self-assembled on silicon substrates.

Molecular-scale devices demonstrated in the lab include FETs, junction transistors and diodes, molecular switches, and mechanical switches. Researchers project densities of 10^{11} to 10^{12} devices/cm^2 [18,24,28]. (In comparison, the 2001 ITRS roadmap for ASICs and MPUs projects $3x10^9$ transistors/cm^2 for 2016 [22].) Nanoelectronic fabrication will be bottom-up batch chemical and physical processes, forming semi-regular arrays with 1% to 5% defect rates. Circuit function will be programmed in and defects programmed around. Cheap gigagate gigabit gigaHertz non-volatile FPGAs and RAMs, built with molecular-scale nanoarrays on silicon substrates, may be in commercial production by 2010-2015.

This paper surveys some recent research results in molecular-scale electronic materials and devices, assembly techniques, and the initial published forays into how we might build systems. This writing is current as of mid-March 2002.

2 MATERIALS AND DEVICES

2.1 System Requirements

Electronic digital systems make some basic demands of devices and interconnects. Active devices must be able to be combined in circuits with logic and storage functions. Signal restoration must make output logic levels match input logic levels. Logic levels need good noise margin and rapid transitions between two states. Fanout and long interconnects require active gain, either in the active devices themselves or else in repeaters. Undesired crosstalk and distortion among wires and devices must be constrained and manageable. Room temperature operation at reasonable power and speed with very high aggregate reliability is essential. Today's digital logic, memory and hardware system architectures can be built on any implementation technology that meets these requirements.

2.2 Carbon Nanotubes

In 1991 Sumio Iijima of the NEC labs discovered a tubular variant of the C_{60} "buckyball" carbon molecule [21]. A carbon nanotube (NT) is a molecular sheet a single atom thick, which has wrapped around into a tube, as little as one nanometer wide and so far up to millimeters long. Since it's a single molecule, nanotubes are extremely strong and flexible (fig. 1).

Depending on their lattice geometry, NTs behave as metals or semiconductors. So far there is no way to synthesize a pure batch of just one type [26]. Some success in selecting NTs by voltage breakdown of undesired types has been reported [8]. Carbon nanotube technology is very new. NTs may become more predictable and manageable in time.

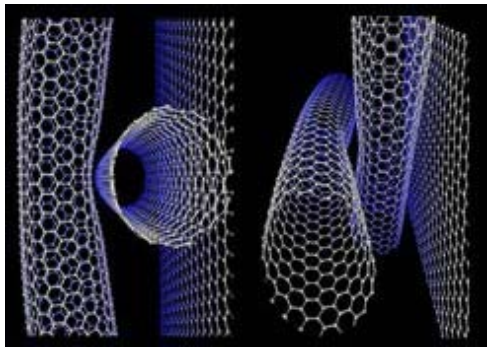

Figure 1: Carbon nanotubes [20]

2.3 Single-crystal Nanowires

Silicon may be the best understood and most manageable of all solids. Single-crystal silicon nanowires (NWs) have been fabricated in bulk by laser-assisted catalytic growth, with diameters of 6 to 20 nm and lengths ranging from 1 to 30 microns (fig. 2. Germanium, gold, gallium phosphide, gallium nitride and indium phosphide NWs have also been made [19,23].

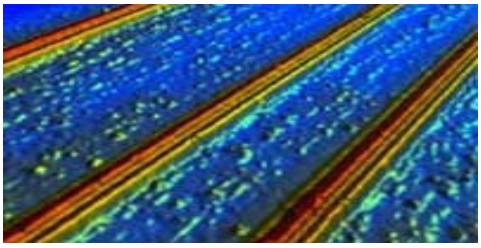

Figure 2: Single-crystal silicon nanowires [28]

Controlled doping of silicon and gallium nitride NWs with phosphorous and boron has been successful, producing p-type and n-type semiconducting nanowires [11].

Both NTs and NWs are used as interconnect wires, or, when doped, as semiconductor devices.

2.4 Transistors and Diodes

Two semiconductor NWs, one p-type and one n-type, form a junction diode at their crossing. Three NWs with two crossings form a junction transistor [10]. Small working NW diode arrays have been made, with 85% to 95% yield, showing independent operation. Turn-on voltages of 1V are observed, and logic gates may be made with CNW(crossed nanowire)-diodes [18] (fig. 3).

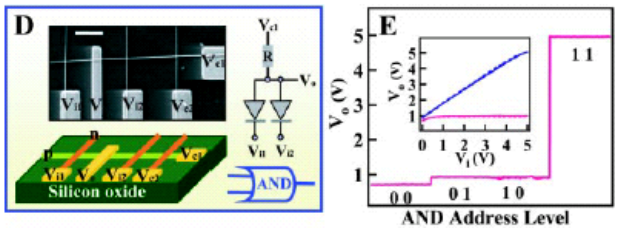

Figure 3: CNW-diode AND gate, V_o-V_i relation [18]

CNW-diodes can be made with 5V turn-on by increasing the oxide thickness at the junctions, by passing high current through a low turn-on diode in air, oxidizing the junction by joule heating [18]. This device is very interesting, as it can be used as a one-time-programmable crosspoint for ROM or logic arrays, or it can be used as an FET (see below).

Many forms of FETs have been reported. One class uses a carbon nanotube as the channel, between contacts over a microscale lithographed gate (fig. 4) [1, 14, 20]. The channel lengths and gates in these devices are microscale, not nanoscale.

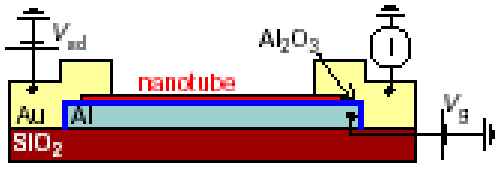

Figure 4: Single-nanotube FET [1]

Bell Labs recently reported FET behavior with only a few organic molecules acting as the channel. Gate bias varies channel conductance by over three orders of magnitude. Quantized conductance behavior confirms the molecular scale of this FET. Though their experimental setup has microscale lithographed gold contacts and silicon gate, this FET behavior through a few molecules is surprising and promising [25].

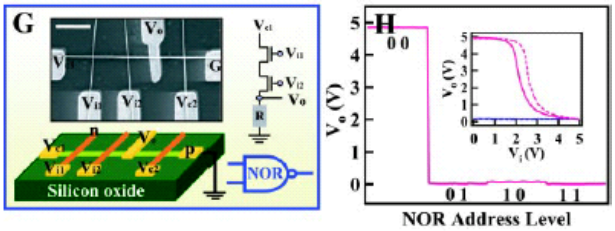

Figure 5: CNW-FET NOR gate, V_o-V_i relation [18]

High turn-on CNW-diodes, cited above [18], act as FETs in their non-conducting region. A p-channel crossed nanowire FET (CNW-FET) has a p-type single-crystal silicon NW channel and n-type single-crystal gallium nitride NW gates. The resulting NOR gate (fig. 5) has a voltage gain of 5 at room temperature. This is the first report of a nanoscale logic gate with gain.

2.5 Molecular Switches

Organic molecules exist which have two mechanically distinct parts, such as a ring and a rod or interlocking rings. Applying a programming voltage across the molecule adds or subtracts an electron (oxidation-reduction), shifting the ring and changing the molecule's conductivity. It's a non-volatile programmable molecular switch.

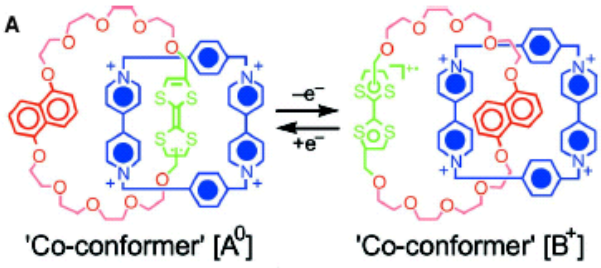

Figure 6: [2]Catenane molecular switch [7]

[2]Catenane (fig. 6) acts as a molecular switch [7]. It opens at 2 volts, closes at –2 volts, and is read at 0.1 volt, and has been cycled open and closed many times. Used between a metal wire and an n-type silicon nanowire, the junction acts as a programmable diode, making an addressable memory array. So far its conductance only varies by 4X between states, so it may

be useful for RAM but not for logic. A nitroamine [3] showed 1000X between states.

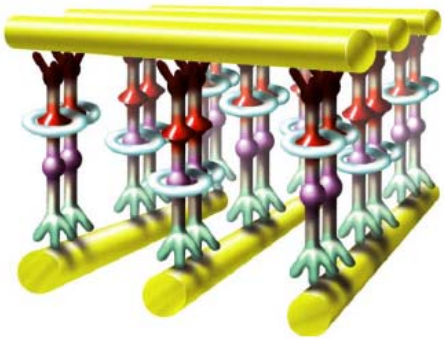

Figure 7: Molecular switches in nanowire crossbar [26]

Fig. 7 illustrates a crossbar with molecular switches of the ring and rod type, such as the rotoxane of [6], which is one-time-programmable. The lower NTs or NWs would be laid down, then the switch molecules applied, then the upper wire layer.

Both these molecular switches and the mechanical switches below have no gain, so signals must be restored between switch arrays by devices with gain, such as CNW-FETs.

2.6 Mechanical Switches

Carbon nanotubes arranged in a crossbar, with the upper half suspended so they are separated from the lower half, will work as a programmable array of non-volatile bistable mechanical switches (fig. 8). Applying enough voltage across a pair of NTs attracts them together, then van der Waals forces keep them in contact, closing a circuit between the NTs. Applying an opposite voltage drives them apart again. This operation was simulated and a single working crosspoint was made [24].

Diodes at the crosspoints are needed for unique addressing without 'backdoor' paths. Using semiconductor NTs or NWs for the lower wires may make diodes at the contact points [24].

Figure 8: Suspended nanotube crossbar switches [24]

3 FABRICATION

Nanowires and nanotubes can be made in quantity [9, 21, 23]. Individual NTs and NWs have been micro-manipulated for device and circuit experiments [24], but that is no good for manufacturing. Masses of NTs and NWs have been made to self-assemble into regular arrays by fluidics [19, 26].

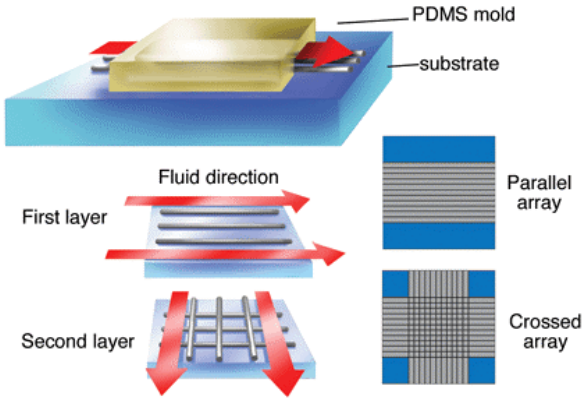

Figure 9: Fluidic channels for nanowire flow assembly [26]

NWs self-assemble into parallel arrays guided by fluid flow (fig. 9). An ethanol fluid carrying NWs in suspension is passed over the substrate guided through a channel in a mold. Average separation can be controlled by varying the flow rate and duration. The NWs adhere well to the silicon substrate, permitting multiple layers to be assembled. Arrays of NWs crossing at right angles have been made this way [19].

Large uniform crossbar arrays are fine for RAMs, but logic blocks in systems need more structure. Crossbar wires can be cut with programming voltage when molecular switches are used at the crosspoints [30]. Applying a high voltage over-oxidizes the crosspoint and breaks the NW, since it's small enough to be consumed by the chemical reaction. This is higher than the voltage used to open or close the crosspoint.

Bottom-up molecular-scale fabrication is universally expected to require defect tolerance due to the nature of chemical processes and alignment at that size. This implies programmable logic (FPGA), tested and programmed to avoid the defects [17].

4 SYSTEM ELEMENTS

4.1 Logic and RAM

Defect tolerance dictates programmable logic. Two-terminal devices are likely, since chemical self-assembly is unsuitable for three-terminal devices. An exception is the two-crossed-NW CNW-FET. Zero leakage power when open must be a consideration at such density. Three candidates have appeared:

1) Mechanical switch with diode. Realization not yet reported. Zero leakage when open, dynamically rewritable.
2) Molecular switch with diode. Rewritable form has too much leakage so far. There may eventually be a one-time-programmable molecule with zero leakage.
3) CNW-diode. One-time-programmable into high turn-on, which is open-circuit with low voltage logic.

These all lack gain, requiring signal restoration, which may be done with integral pipeline registers [15], possibly using CNW-FETs. They are all non-volatile, a major asset for logic as well as for RAM. Molecular and mechanical switches are the best rewritable candidates for RAM so far.

4.2 Interface to Microelectronics

Nanoelectronics must have an interface to microelectronics to be useful. Top-down photolithographed silicon will remain the substrate, providing mechanical support, packaging and PCB pins, as well as remaining the medium for analog and interface electronics. Nanometer-scale nanowires must be connected to sub-micron-scale microwires somehow. Two possibilities have been proposed, but not realized, so far. Both implement binary decoders which connect N nanowires to log(N) microwires.

Figure 10 shows 2 log(N) nanowires attached to an orthogonal set of microwires, and decoded into N nanowires by a true/complement AND array with a patterned binary mask [13]. Where the pattern leaves openings between nanowires, the crossover forms FETs, whose channels are the decoded nanowires. Such a pattern between the nanowire layers could be formed with a nanoscale stamp imprint [4,5]. This imprint has nanoscale features but can only be positioned with microscale accuracy, so some extra nanowires are included to provide slack. Even N=1000 nanowires needs only 10 microwires, so the nanoscale array can match up with microscale interfaces.

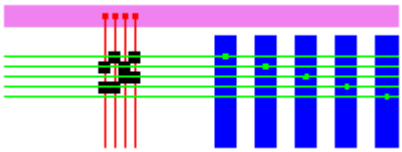

Figure 10: Patterned mask micro/nano decoder [13]

Figure 11 shows a similar micro/nano decoder, but here the microwires and nanowires are interconnected by randomly distributed gold nanoparticles. The particles are sized and concentrated so 50% of the microwire/nanowire crossovers are connected. Using about 4 log(N) microwires insures that enough will turn out, after testing, to completely and uniquely address enough of the nanoarray [28,29].

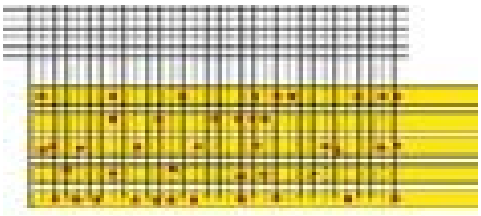

Figure 11: Random particle micro/nano decoder [28]

4.3 Large Defect-Tolerant Systems

In the mid-1990s HP Labs built a reconfigurable computing system called Teramac [12], which addressed defect tolerance in large programmable hardware systems. Teramac had 8 boards, with 4 MCMs each, and 27 custom FPGAs per MCM. 75% of the FPGA die, 50% of the MCMs, and 10% of the inter-chip signals were defective. They found methods for detecting defects at all levels of logic and interconnect, and using FPGA programmability to compile around them, and achieved years of reliable operation [17].

4.4 System-level Interconnect

DeHon [13], Goldstein's CMU group [15], and HP Labs [30] have started investigating how systems would be built from nanoscale crossbar arrays. Logic could be in programmable OR or NOR arrays like today's PLAs, only much larger, probably segmented by wire cutting.

Having programmable crosspoints that fit into the wire overlap area means fully connected crossbars are economical. There is no need to partially populate them to save area as with today's CMOS FPGA architectures, which must trade flexibility and utilization for area. Full routing richness makes compilation much easier. It makes defect tolerance reasonable as well.

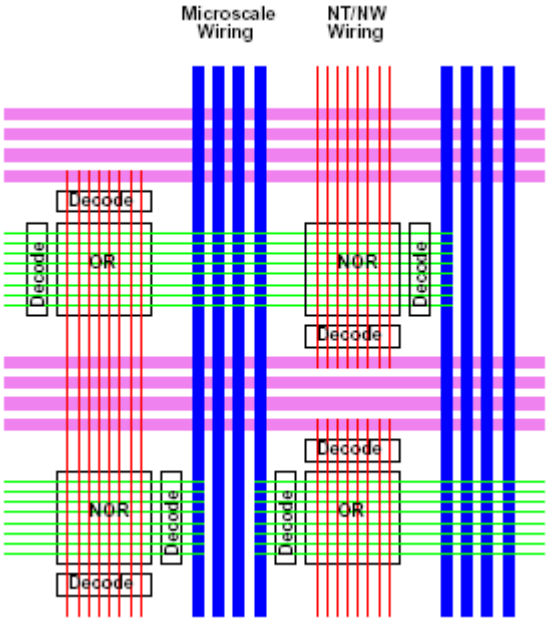

Figure 12: System of logic arrays (not to scale) [13]

Logic arrays can be interconnected by extending NWs across multiple arrays (fig. 12), or by crossing over through programmable interconnect crossbars. CNT-FET signal restoring pipeline registers may be placed in the interfaces [15].

5 TECHNOLOGY PROJECTIONS

5.1 Area: MicroASIC vs. NanoFPGA

The area of an FPGA is almost entirely determined by the area of its programmable crosspoints. Current technology uses about 20 crosspoint cells per ASIC gate-equivalent of logic, including interconnect. In microscale CMOS, a typical crosspoint cell is a 5T or 6T SRAM bit and a large n-channel pass transistor. This takes much more area than the minimum wire pitch squared, so device area determines FPGA logic density. Table 1 shows FPGA gate densities for a range of ITRS 2001 roadmap geometries [22], assuming 8 transistors' area per crosspoint cell.

Mechanical and molecular NT programmable crosspoints fit in the same area as the wire crossovers. So logic and memory area is determined by the wire pitch. Table 2 shows some hypothetical nanoscale crosspoint cell densities and gate

densities, assuming 20 crosspoints per gate, and 20%, 50% or 80% utilization of the raw cells due to defect avoidance and other overheads.

Table 1: Density of microchip FPGA crosspoints and gates

Year	Process	xstr/cm^2	cells/cm^2	gates/cm^2
2001	150 nm	89 10^6	11 10^6	0.6 10^6
2004	90 nm	178 10^6	22 10^6	1.1 10^6
2007	65 nm	357 10^6	45 10^6	2.2 10^6
2010	45 nm	714 10^6	89 10^6	4.5 10^6
2013	32 nm	1.4 10^9	180 10^6	8.9 10^6
2016	22 nm	2.9 10^9	360 10^6	18 10^6

Comparing tables 1 and 2, we see a nanoelectronic FPGA with 50 nm wire pitch (about 10X nanowire thickness) and 20% utilization, would have 400 million gates per cm^2, 20X the gate density of the 22 nm CMOS FPGA of 2016. 25 nm pitch and 50% utilization is 10X better, 4 billion gates, and 10 nm pitch at 80% utilization is another 10X, 40 billion gates.

Table 2: Density of nanochip FPGA crosspoints and gates

Wire pitch	cells/cm^2	gates/cm^2 20% util.	gates/cm^2 50% util.	gates/cm^2 80% util.
50 nm	40 10^9	400 10^6	1 10^9	1.6 10^9
25 nm	160 10^9	1.6 10^9	4 10^9	6.4 10^9
10 nm	10^{12}	10 10^9	25 10^9	40 10^9

Table 3 shows microchip ASIC gate densities, at 4 transistors per gate and ITRS 2001 figures. The 50 nm pitch 20% utilized nanochip FPGA has the same density as the ASIC of 2013. At 10 nm pitch and 80% utilization it would be 50X denser than the 2016 ASIC, 40 billion gates per cm^2.

Table 3: Density of microchip standard cell gates

Year	Process	xstr/cm^2	gates/cm^2
2001	150 nm	89 10^6	22 10^6
2004	90 nm	178 10^6	45 10^6
2007	65 nm	357 10^6	89 10^6
2010	45 nm	714 10^6	180 10^6
2013	32 nm	1.4 10^9	360 10^6
2016	22 nm	2.9 10^9	720 10^6

5.2 Speed, Power

While individual nanoscale devices may switch at over 100 GHz [24], wiring will determine nanoarray speed. [30] contains a first-order estimate of NT wiring's RC time constant, and predicts 1 GHz or better for arrays.

Power may or may not be a difficult, even fatal, problem. At 10^{11} devices/cm^2, one nanowatt per device results in 100 W/cm^2. Leakage could dominate. While CNW-FETs have shown three orders of magnitude conductance range, programmable molecular switches reported so far only have a 4X range. Zero leakage when off may be required. The mechanical switch clearly offers that, and one-time-programmable molecular switches may eventually as well. CNT-FETs remain to be seen.

5.3 Development Roadmap

The first practical nanoelectronic devices are likely to be nonvolatile RAMs, since they are regular arrays and defect tolerance is already normal. Nanoarrays with 30 nm pitch would have 10^{11} crosspoints (10 GBytes) per cm^2. 10 nm pitch would yield 100 GB/cm^2. Press reports say Heath's UCLA team made a 16-bit memory using molecular switches in 2001, and HP Labs has a 16 Kbit goal for 2005. Kuekes and others see commercial niche application emerging soon after that, catching up with microscale CMOS density around 2011.

Programmable logic array development should parallel RAM progress. Catching up with CMOS FPGA density may come sooner, thanks to the radically smaller programmable crosspoint. After about 2013 the densest logic technology of all would be the nanoscale FPGA, surpassing microelectronic CMOS. All state-of-the-art digital electronics would by then be shifting into field programmable nanoarrays. Multi-billion dollar fabs would be replaced by less expensive nanoarray fabs. Silicon photolithography would stabilize at a constant set of design rules and fabs will have long lifetimes as substrate providers.

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